Progress in screen printed front side metallization schemes for CSiTF solar cells

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ABSTRACT

The Buried Base Contact (BBC) concept represents a simple industrially feasible scheme for metallizing crystalline silicon thin film (CSiTF) solar cells on insulating substrates and further allows metallization by screen printing. However, cells suffered from fill factors of ~ 50 % due to R_s and R_p losses. By evaluating Al and AgAl pastes for base contacts, R_s is reduced below 1.5 Ωcm². Improved definition of base regions and improved alignment results in shunt resistances > 1 kΩcm². The interdigitated cells processed on Cz-Si wafers show fill factors up to 73 % and efficiencies of 11.5 %. Implementation of a firing through SiN_x sequence is difficult due to the formation of inversion channels between emitter and the base grid and R_s problems. An extended BBC process scheme is proposed, which allows an integrated interconnection of CSiTF cells on one substrate. However, the application to CSiTF leads to significant difficulties due to surface roughness of the substrates.

INTRODUCTION

The need for cost reduction in production forces the PV industry to develop more cost effective solar cell and production schemes. One promising concept to reduce material costs is the crystalline silicon thin-film (CSiTF) solar cell [1]. In contrast to conventional solar cells, the base of a CSiTF solar cell can be contacted from the rear side only if the substrate is conducting. Otherwise, both contact grids have to be applied on the front side. A lot of research has been done on CSiTF cells on foreign substrates leading to maximum efficiencies of 10.8 % on insulating substrates and 11.0 % on conducting substrates [2] based on laboratory-type solar cell processes. A more industrially relevant process scheme, the screen printed Buried Base Contact (BBC) concept has been developed at Fraunhofer ISE reaching conversion efficiencies of 7.6 % on 300 μm thick mc-Silicon [3].

The aim of this work has been a further development of the BBC process scheme with respect to higher fill factors. This led us focus on the properties of the screen printed base contacts with respect to fine line printing, low line and specific contact resistance and improved alignment of the base grid. Based on these results a new interdigitated grid has been designed. Finally, an extended process scheme for integrated interconnection of several thin film solar cells on one substrate is proposed.

EXPERIMENTAL

All cells were fabricated on *p*-type Cz-Si wafers with a bulk resistivity of ~ 1 Ωcm. Wafer thickness before damage etching was about 330 μm. Details of the fabrication process are given in [3]. The main process steps are shown in Figure 1. After saw damage removal and cleaning the formation of the *n*-type emitter leading to a sheet resistance of ~ 35 Ω/sq was carried out in an infrared heated conveyor belt furnace.

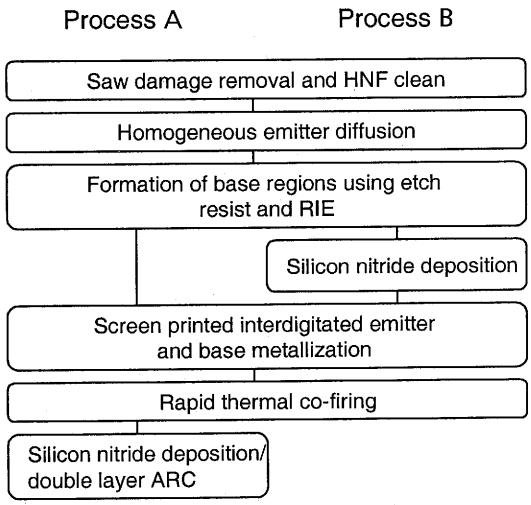

Figure 1: Process sequences for the BBC concept used in this work.

As an etching mask for RIE a screen printable etch resist has been used. The width of the designated base regions was varied between 300 and 400 μm, bearing in mind the limitations of the screen printed contact fingers. Approximately 3 μm of the silicon surface including the emitter layer were removed by low-damage RIE in a SF_6-plasma. Afterwards the etch resist was stripped using acetone. To include a firing-through silicon nitride process, the run was split up. For the firing through experiments, the passivating SiN_x layers have been prepared by PECVD in a conventional parallel plate direct plasma reactor [4].

The base contacts were screen printed prior to the emitter grid due to enhanced alignment requirements for base regions and base contact grid. For the base contacts we used commercially available aluminium and

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aluminium-silver pastes, for the emitter contacts a silver paste. Aligned screen printing has been performed using a screen printer with optical alignment system. The alignment was carried out by adjustment marks or edge detection, respectively. On the back side of the cells an aluminium paste was screen printed in order to create an effective back surface field. The cells were co-fired by means of Rapid Thermal Firing, applying an optimized process [5]. On the front side of the cells without firing through, a double layer antireflection coating was deposited after complete metallisation. All interdigitated cells have been compared with conventional screen printed solar cells.

EVALUATION OF BASE METALLIZATION PASTES

So far, the low fill factor was due to the poor matching between base region and base contacts as well as the conductivity of the base fingers (see [3]). This originated from shunts caused by an unsuitable printing behaviour of the Al paste as the paste is daubed during printing. In addition, series resistances > 6 Ωcm^2 were found due to interruptions in the base contact.

Having these results in mind, we focused on improving the definition of the base region combined with improving the printing behaviour of the base metallization. Our objective was to find a more suitable paste fulfilling the following requirements: (1) fine line printing ability, (2) low contact resistance, (3) low line resistance.

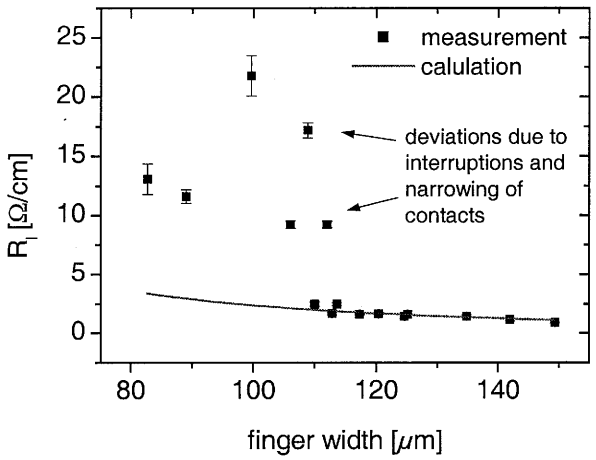

Figure 2: Typical line resistance as a function of finger width. The calculation is based on the measured finger geometry and the paste resistivity after firing.

We tested several pure Al pastes as well as two different AgAl pastes on *n*-type Cz silicon material with a boron diffused emitter with a non-passivating SiN_x ARC layer applied. From the results for both kinds of paste, line resistances are approximately 3 times higher (R_l ~ 1.5 Ω/cm) than typical values for pure Ag pastes, which compares well with results in [6]. No improvement in line conductivity has been found when using AgAl instead of Al pastes. From the results of the paste evaluation a pure Al paste turned out to be the best compromise between low resistivity ($\rho \sim 2 \cdot 10^{-7}$ Ωm), leading to a low line resistance (R_l ~ 1.5 Ω/cm) and a low contact resistivity ($\rho_c \sim 2.5 \cdot 10^{-4}$ Ωcm^2) on a non passivating SiN_x layer. Furthermore, the paste allows printing fine lines reproducibly down to a width of around 120 μm (Figure 2) with sufficient electrical properties.

RESULTS ON SILICON WAFERS

Based on the paste evaluation a new interdigitated grid has been designed as to minimize ohmic and optical losses due to both contact grids. The calculations have been carried out analytically based on modified standard formulae. Ohmic losses due to a lateral current flow in the base have been considered by a sheet resistance $R_{sh,\ base}$. Recombination and 3-d current flow have been neglected. A picture of the cell design is shown in Figure 3. Boundary condition for the optimum cell size was 4 x 4 cm^2, therefore the optimal length of a contact finger was 1.3 cm and the optimal distance between the contact fingers turned out to be 3.3 mm. The possibility for further upscaling towards larger areas and an implementation into a 4 x 4 cm^2 module on a CSiTF substrate is given.

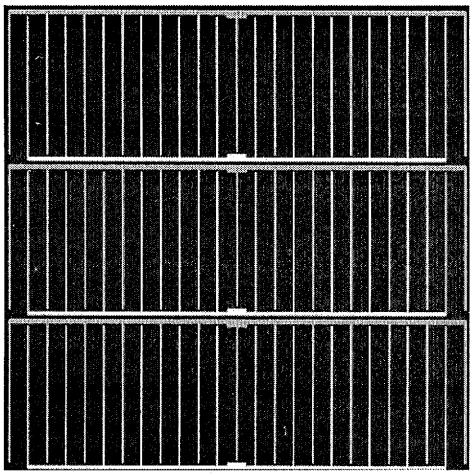

Figure 3: Cz-Si solar cells with interdigitated front grid developed within this work (subcell size 13 x 40mm^2).

Table 1 shows the result of process optimization (Process A). The mean values of the processed BBC solar cells are shown. Small deviations of the mean value in each solar cell parameter indicate a very stable solar cell process.

Table 1: Mean solar cell results without AR coating (average of six cells).

	V_{oc} [mV]	I_{sc} [mA/cm^2]	FF [%]	η [%]
BBC	585±0.2	18.7±0.1	73.4±0.5	8.1±0.1
Standard	601±0.7	22.7±0.1	75.8±0.1	10.3±0.1

Results of the best cells with and without firing through process applied are shown in Table 2. A double layer antireflection coating has been applied after the metallization for the cells with no firing through process. Concerning V_{oc} values, the gap between a cell with interdigitated grid and a standard cell can be decreased by firing through a well passivating SiN_x layer, as shown in Table 2. However, V_{oc} is still reduced by ~ 10mV.

Table 2: Best solar cell results obtained so far with no firing through (FT) and firing through process.

Process	V_{oc} [mV]	I_{sc} [mA/cm²]	FF [%]	η [%]
no FT	596	26.5	73.2	11.5
FT	603	28.9	53.5	9.3
Standard	613	30.2	77.5	14.3

Short circuit current densities of 26.5 mA/cm² have been measured for the interdigitated grid cells. This value reflects the inactive cell area of 20 % due to surface recombination in the base regions surrounding the base contacts as well as shadowing. LBIC-mappings confirm the very low current collection in this region (Figure 4, left). For the firing through cells the short circuit current increases significantly compared to the no firing through process. This can also be confirmed by the LBIC mapping of such a cell (Figure 4, right), where the unpassivated open base area is obviously reduced.

A fill factor of 73.2 % is reached, resulting in a cell efficiency of 11.5 %. By comparing the dark with the light IV-characteristics series resistance values of 1.6 Ωcm² could be achieved. The shunt resistance values increase up to values of $2 \cdot 10^4$ Ωcm² for a base region width of 360 μm.

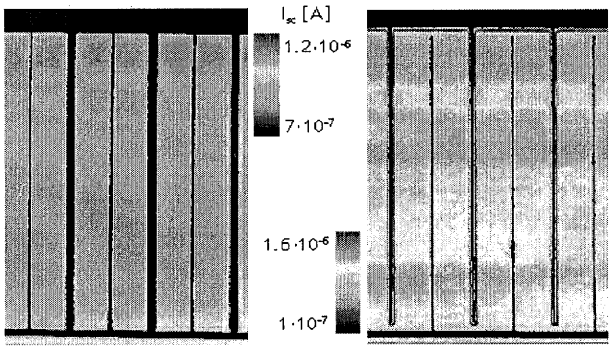

Figure 4: LBIC mappings of cells without firing through (left) and with firing through (right) process (measured at wavelength of 790 nm).

For the firing through experiments, both types of conductor pastes (pure Al and AgAl) for the base metallization have been tested. In contrast to the paste evaluation, the process is not successful using the Al paste when the passivating SiN_x layer is present. The layer may act as a barrier to Al alloying with the underlying Si lattice [7]. As a result, the Al grid printed on SiN_x can be easily wiped away after the firing process.

Results are different for the AgAl paste. This paste shows the ability to punch-through the SiN_x layer, which is aided by the higher glass frit content. But the cells performance is obviously limited by a very low fill factor. These values cannot be explained by shunting problems due to a bad printing alignment. In fact, the cells show a series resistance R_s of 6 Ωcm², comparing the dark and light IV characteristics. This value can be explained by an increased contact resistance to the underlying Si material for firing through the passivating SiN_x layer.

The fill factor is badly influenced by a hump of the dark IV characteristic (Figure 5) in the region of the maximum power point (0.4-0.55 V). This can be explained by the formation of inversion channels beneath the SiN_x layer [8].

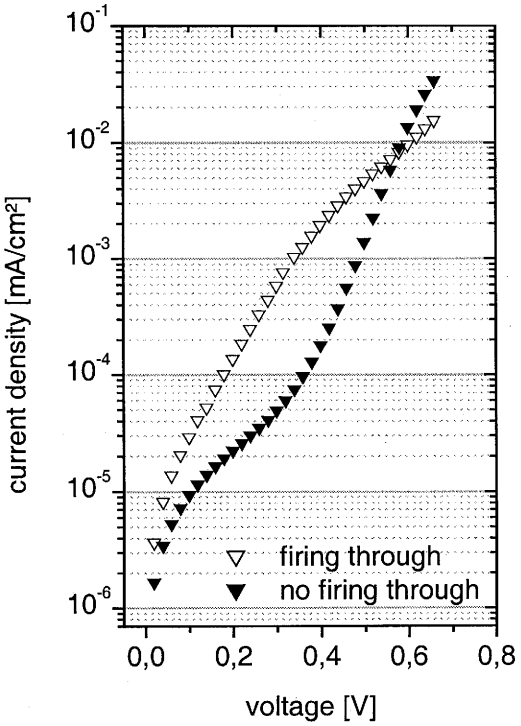

Figure 5: Dark IV-characteristics of solar cells with and without firing contacts through a passivating SiN_x layer.

APPLICATION TO CSiTF SOLAR CELLS

The transfer of the BBC concept to CSiTF cells requires some extensions with respect to series interconnection [3]. For a monolithically series connection of adjacent cells on one isolating substrate, a separation step is needed. This step can be included in the process scheme directly after emitter diffusion. The surface damage caused by the cutting step is then removed by the following plasma etching steps. In addition, after the metallization a connection has to take place to ensure the monolithically interconnection of the cells.

A thermally grown SiO_2 layer on *p*-type Cz silicon (bulk resistivity ~ 1 Ωcm) has been used as substrate. Thereon a *p*-type seeding layer has been deposited. After recrystallization a double layer deposition has taken place to build up the active Si layer. Afterwards the cells have been processed using the same solar cell process scheme described above.

During the processing of the samples, some major drawbacks of CSiTF in conjunction with the screen printing process could be identified (see also [9]).

As a result of the surface roughness severe problems in the definition of the structure arise at steps on the wafer surface as they lead to slumping of the Al paste as well as of the etch resist (Figure 7).

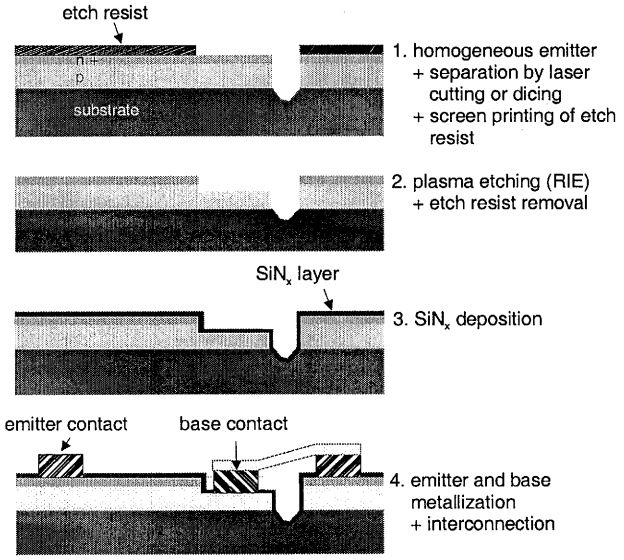

Figure 6: Process scheme for the monolithically series interconnection of cSiTF solar cells

Due to these effects the BBC cells suffer from increasing leakage currents. Furthermore, the etching of the trenches for the base grid via RIE is noticeably inhomogeneous, depending on the grain structure of the epitaxially grown silicon layer. As a result of these difficulties, the application of the BBC concept to CSiTF substrates still requires larger efforts.

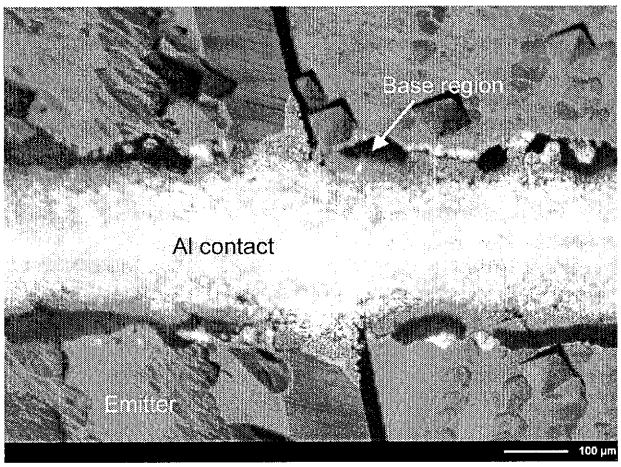

Figure 7: Base metal finger on an epitaxial grown crystalline silicon layer. The slumping of the paste at surface steps can be seen clearly.

CONCLUSION

An industrially feasible interdigitated emitter and base front side metallization scheme for CSiTF cells with series interconnection based on the BBC concept is presented. On Cz silicon wafers efficiencies up to 11.5 % could be achieved, applying a double layer antireflection coating after the metallization step. With a firing through process, cell efficiencies are still limited to 9.3 %, however, with high open circuit voltages up to 603 mV and short circuit currents up to 28.9 mA/cm². These cells were limited by a decreased fill factor due to significantly higher series resistance values of more than 6 Ωcm^2 and the formation of inversion channels between the SiN_x and the emitter layer.
Transferring this concept to crystalline silicon thin film substrates still causes problems mainly due to steps at the surface of the epitaxially grown thin silicon layer. For process stability self aligned process schemes have to be considered to overcome the alignment difficulties of screen-printed base contact grids in one side contacted solar cell process schemes.

ACKNOWLEDGEMENTS

The authors would like to thank E. Schaeffer and G. Emanuel for technical assistance. This work was supported by the European Commission in frame of the SUBARO project (Project-No. NNE5-1999-00332), also by the Federal Ministry of Economics and Technology under contract no. 0329836 (TEKSI). D.M. Huljic is supported by the scholarship program of the Deutsche Bundesstiftung Umwelt, Germany, and a scholarship of the Albert-Ludwigs-University Freiburg, Germany.

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