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Atmospheric Pressure Dry Etching of Polysilicon Layers for Highly Reverse Bias-Stable TOPCon Solar Cells

Bishal Kafle, Sebastian Mack, Christopher Teßmann, Sattar Bashardoust, Laurent Clochard, Edward Duffy, Andreas Wolf, Marc Hofmann, and Jochen Rentsch*

Single-sided etching (SSE) of a-Si/poly-Si is typically considered a challenge for realizing a cost-efficient TOPCon production sequence, as there is a certain degree of unwanted wrap-around for poly-Si deposition technologies such as low pressure chemical vapor deposition, plasma-enhanced chemical vapor deposition, and atmospheric pressure chemical vapor deposition. To date, alkaline or acidic wet-chemical solutions in either inline or batch configurations are used for this purpose. Herein, an alternative SSE process is proposed using an inline dry etching tool, which applies molecular fluorine as the etching gas under atmospheric pressure conditions. The developed etching process performs complete etching of both as-deposited amorphous silicon and annealed polycrystalline silicon layers, either intrinsic or doped, and with measured etch rates of $>3\ \mu m\ min^{-1}$ at 10% F_2 concentration allows etching of a typical layer thickness of 200 nm in just a few seconds. The etching process is also configured to perform excellent edge isolation while maintaining a low wrap-around etching ($d_{rear} < 500\ \mu m$) at the opposing-side. The etching process is successfully transferred to the industrial TOPCon solar cell architecture, yielding high parallel resistances ($S_{shunt,avg.} > 1500\ k\Omega\ cm^2$), low reverse current density ($J_{rev,avg} < 0.8\ mA\ cm^{-2}$) measured at a bias voltage of −12 V, and independently certified conversion efficiencies of up to 23.3%.

1. Introduction

Photovoltaics (PV) industry is currently looking at different cost-effective manufacturing options of transferring the tunneling oxide passivated contacts (TOPCon) concept into production, especially keeping in mind a strong competition from state-of-the-art *p*-PERC cells in terms of process reliability, cost of ownership, and levelized cost of electricity. The efficiency potential of TOPCon-based solar cell architecture concept is already proven in laboratory scale solar cells by reaching V_{OC} of up to 725 mV and conversion efficiencies of 26.0% and more.[1,2] Moreover, initial industrial adaption of this technology by PV manufacturers also shows promising results.[3–5] Low pressure chemical vapor deposition (LPCVD) is currently the mainstream amorphous/polycrystalline silicon layer (a-Si/poly-Si) deposition technology used to fabricate industrial TOPCon cells.[6,7] Apart from high deposition rates, LPCVD allows in-situ thermal oxidation of crystalline silicon (c-Si) surface to form a tunnel oxide before deposition of poly-Si layers in the same tube. However, since a-Si/poly-Si layer is inherently deposited on both sides of the wafer, a single-sided etching (SSE) of this layer is required on the front side for typical TOPCon configuration in n-type substrate, where the TOPCon layer is placed at the rear-side of the cell. The SSE process should not only minimize the optical losses arising due to a strong absorption of incident light by the poly-Si layer, but also avoid the formation of shunts in the wafer and the wafer-edges, or alternatively, remove such shunts, if they are present in the samples. Among competing deposition methods, SSE is typically also performed for plasma-enhanced chemical vapor deposition (PECVD)-deposited layers as a complete single-sidedness is not achieved even for the deposition of thin (30 nm) poly-Si layers;[8] whereas absolute single sidedness of atmospheric pressure chemical vapor deposition (APCVD) technique was not realized in the literature.[9] Physical vapor deposition (PVD) is reported to provide single-sided poly-Si deposition;[10] however, an industrial process is still under development.[7,11]

In industrial TOPCon cells, SSE is reportedly performed in a wet-chemical process using either alkaline solution (KOH/NaOH), acidic mixture of HF/HNO_3 and HF/DIO_3, or their combinations.[12,13] The current SSE methods, however, suffer from low etch rates (ERs) and low batch-to-batch reproducibility. Apart from that, additional use of wet chemicals, especially HF/HNO_3, is preferably kept low in large-scale manufacturing due to the costs related to the process consumables and the abatement processes.

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In this work, we propose an atmospheric pressure dry-etching (ADE) process[14] to perform single-sided etching of amorphous/polycrystalline silicon (a-Si/poly-Si) layers for fabrication of industrial TOPCon solar cells on n-type substrates. The process uses diluted molecular fluorine (F_2) as the etching gas to enable high throughput inline etching of silicon layers in atmospheric pressure conditions, avoiding the need of ion induced excitation. We first start discussing the etching property of the a-Si/poly-Si layer and aim to devise TOPCon cell processing routes to incorporate the ADE process in the cell processing flow. Using cell-like precursors prior to metallization, detailed microscopic investigations are used to discuss the progression of a-Si/poly-Si etching on the front side, which is followed by the investigation of the rear-side wrap-around and edge isolation. Finally, we present results of first bifacial TOPCon solar cells featuring the developed SSE process and discuss about the reverse bias property of the fabricated solar cells.

2. Single-Sided Etching of Polysilicon Layer

2.1. Etching Tool

The single-sided etching process is performed using the ADE tool, which previously has been used extensively for etching and texturing of crystalline silicon (c-Si) surfaces.[14]

The schematic of the process is shown in **Figure 1**.

Here, c-Si wafers are loaded in a heated conveyer belt using an automation tool and transported through the reaction chamber in an inline fashion. The etching gas (F_2/N_2 gas mixture) flows through a heated ($T_{GDP} = 200$–$300\,^{\circ}C$) gas diffusion plate (GDP) into the reactor, which is kept effectively at atmospheric pressure conditions. As there is no plasma or reactive ion involved in the etching process, the process solely depends upon the thermal activation of F_2 directly at the silicon wafer surface that facilitates chemical reaction of fluorine species with the deposited silicon layer on the c-Si wafer substrate, which is heated to moderate temperatures of $T_{wafer} = 200$–$250\,^{\circ}C$. The reaction products are transported away through the exhaust into a dry scrubber in our laboratory setup, which can be replaced, for example, by a wet scrubber in an industrial scenario. More details about the etching tool and its use in c-Si etching can be read in previous studies.[14–16]

2.2. Etching Property

To investigate the etching characteristics of the a-Si/Poly-Si in both as-deposited and annealed states, etch thickness and ERs are measured after varying the tool process parameters. A detailed analysis using design of experiments (DOE) is performed in parallel, the results of which will be discussed separately due to being beyond the scope of this article. For current study, half-etched fabricates were used to estimate the etch depths and the ERs. The results are shown in **Figure 2**.

For the experiment, n-type, saw-damage etched c-Si wafers are used as precursors. After wet-chemical cleaning, a thermal oxide layer (90 nm) is grown before depositing either intrinsic amorphous silicon (a-Si(i)) layer (160 nm) or in situ phosphorous-doped polysilicon (poly-Si(n)) layer (200 nm) in the LPCVD furnace. The task of the thermal oxide is to act as an etch stop during ADE and to enable thickness measurements of the deposited polysilicon layers. Intrinsic a-Si(i) layers are subjected to a $POCl_3$ diffusion process that simultaneously leads to phosphorous doping and crystallization of the amorphous layers into polycrystalline silicon (poly-Si(n)) in a so-called $POCl_3$-anneal process. After a short HF dip (2%HF, 2 min), the precursors are passed through the ADE etching chamber with a preconfigured gas flux (F_2 concentration = 10%), temperature and speed ($v = 23\ mm\ s^{-1}$). When one-third of the wafer length has entered inside the etching zone, the gas flow is abruptly stopped so that the different positions of the wafer are exposed to the etching gas for different durations. This allows the determination of the etch depth for this test setup. Cross-sectional scanning electron microscopy (SEM) imaging (Zeiss Auriga 60) is used to estimate the layer thicknesses (20 points) on the etched and unetched (rear) sides of the sample to calculate the etch depth.

For calculating the etching duration for each position, we assigned a process starting position ($t = 0$ s) on the wafer by looking for the furthest point from the wafer edge with no apparent

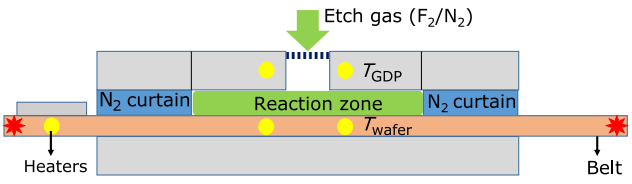

Figure 1. Schematic showing ADE tool used for the etching experiments. Here, T_{GDP} and T_{wafer} represent set-temperatures of the gas diffusion plate and Si wafer moving dynamically in a heated belt, respectively.

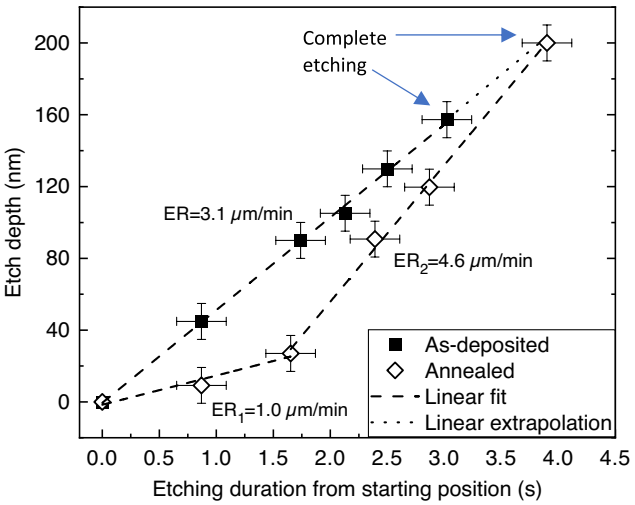

Figure 2. Plot showing etch depth and associated ERs for as-deposited in situ phosphorous-doped and annealed ex situ phosphorous-doped LPCVD deposited silicon layers. Here, the dashed line represents the linear fit of the dataset, the dotted line represents linear extrapolation of data points. The blue arrows show the data points where complete etching of layers is achieved. Apparent ERs are also shown for as-deposited (ER) and annealed (ER_1 and ER_2) layers. ER, ER_1, and ER_2 are calculated from the respective slopes of the linear fits. ER_1 and ER_2 represent the intermediate ERs, whereas ER represents total ER.

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etching of a-Si/poly-Si layer based on visual inspection and SEM investigation. Error bars are included to reflect the inaccuracy in distance measurement (±5 mm), which is translated to the process duration (X-error). Inaccuracy in estimation of layer thickness from cross-sectional SEM measurements is assumed as Y-error = ±10 nm.

It is observed that the etching starts faster in case of as-deposited layers in comparison with the annealed layers. The etch depth increases linearly with the process duration for the as-deposited layer, indicating a quasiconstant ER. In contrast, there are distinctly two etching regimes for the annealed layer—first with a slower etching rate ($ER_1 = 1\ \mu m\ min^{-1}$) and second with higher ER ($ER_2 = 4.6\ \mu m\ min^{-1}$). In fact, ER_2 exceeds the total ER achieved with as-deposited layer ($ER = 3.1\ \mu m\ min^{-1}$). With increasing process duration, etch depth of annealed layer seems to steadily increase in linear fashion to converge with the extrapolated data for as-deposited layer. Note that, for annealed layers, the SEM measurements underestimate the etch depth and ER values, as it does not consider the increase in porosity of annealed poly-Si layers with increasing process duration (see Figure 4 in Section 2.4).

In Figure 2, a slower etching at the start of the annealed layers can possibly be attributed to a high selectivity of F_2 gas to silicon in comparison with the native oxide layer.[14] Although HF dip was performed after LPCVD deposition, even a short waiting time (≈30 s) after HF dip is reported to grow native oxide layer on c-Si surface.[17] The experimental conditions in our experiments are similar, where the waiting time between HF dip and ADE process is even much longer (up to 1 h). Meanwhile, studies by Oshaki et al. show that native oxidation of amorphous silicon layers also occur in ambient air at room temperature.[18] Nevertheless, the oxidation phenomena might differ in case of amorphous and crystalline silicon layers. In amorphous silicon layers, oxygen atoms are reported to readily diffuse into the layer resulting in the oxygen incorporation not only on film surface but also inside the film.[18] This might lead to a constant etching rate of in situ doped amorphous silicon layers in our study. Nevertheless, more research is required to understand the exact role of oxidation on etching behavior of F_2 in amorphous and polycrystalline silicon layers.

Meanwhile, for annealed layer, the second etch regime showing quasiconstant ER (ER_2) that is higher than the ER of amorphous layers (ER) suggests an additional factor influencing the ER. It is suspected to be linked to the different structural nature of the annealed layer (single crystals with grain boundaries), which leads to different progression of etching in comparison with the as-deposited layer. This will be briefly discussed later in the Section 2.4. In summary, high ERs $>3\ \mu m\ min^{-1}$ could be reached for both layers with the applied process parameters, which could be further increased at higher F_2 flows and concentration. In addition, increasing process temperature is also known to exponentially increase the silicon ER,[14] which suggests further potential in increasing the process throughput and lowering the process costs in high volume manufacturing. However, even with the process utilizing 10% F_2 concentration at 225 °C, the deposited silicon layer of around 200 nm thickness can be etched in just a couple of seconds. Note that the exact value of ERs calculated here using half-fabricates on saw-damage etched (SDE) surfaces are likely to vary from the full area etching of textured cell precursors due to following reasons: 1) prolonged etching of half-etched fabricates due to remaining F_2 in the reactor, even after switching mass flow controllers (MFCs), can cause error in approximation of the starting point ($t = 0$ s), 2) higher surface area of textured surface could require longer process duration in comparison with flat surfaces. In fact, we achieved complete etching of 180–200 nm-thick polysilicon layer in M2 size ($A = 244.3\ cm^2$) textured and diffused solar cell-like precursors (rear-side after chemical edge isolation) in <6 s at $T_{wafer} = 225$ °C and F_2 concentration = 10%, whereas in <3 s at $T_{wafer} = 245$ °C and F_2 concentration = 30%, depending upon the used F_2 flux. This suggests an ER of 1.5–4.5 $\mu m\ min^{-1}$ depending upon applied ADE process conditions. In comparison, the literature on wet-chemical etching of poly layer reports an effective ER of ≈0.3 $\mu m\ min^{-1}$ for NaOH solution,[19] whereas ≈0.36 $\mu m\ min^{-1}$ for a two-step etching process using HF-HNO_3 followed by KOH.[13]

2.3. Integration in TOPCon Solar Cell Processing Flow

Figure 3 schematically shows two different TOPCon processing routes based upon LPCVD a-Si deposition technology. The process flows are also accompanied by the schematic cross-section of solar cell precursors at the important steps to facilitate the understanding of the requirements for a wrap-around removal process. Note that the two example process routes are designed mainly for demonstration of applicability of ADE process on both in situ or ex situ doped polysilicon layers, resulting in low reverse current densities. Leaner process flows with higher efficiency potentials are currently being investigated and will be discussed in future studies.

Here, the two TOPCon routes differ mainly by the method used to form doped a-Si/poly-Si layers. For both routes, boron doping is performed on alkaline textured surfaces using BBr_3 precursor in a tube diffusion furnace to form boron (p^{++}) emitter. This is followed by a chemical edge isolation (CEI) process to perform single-sided removal of rear-side emitter, whereas keeping the BSG layer in front-side intact before performing the cleaning sequence. This provides a wide process window that can be used for the a-Si/poly-Si etching process.

Afterward, tunnel oxide is formed in situ by oxidizing c-Si surface inside LPCVD furnace, which is followed by deposition of either intrinsic (TOPCon_ex situ) or phosphorus (n^+-) doped a-Si/poly-Si layer (TOPCon_in situ) process. The LPCVD a-Si/poly-Si deposition by LPCVD is inherently both-sided, therefore leading to a parasitic deposition of layers on the undesired (front) side. For the ex situ route, a $POCl_3$-anneal process is performed at high temperature ($T = 800$–900 °C) to incorporate dopants into a-Si/poly-Si layer, which simultaneously acts as a thermal annealing step required to cause phase change of predominantly amorphous layer to a polycrystalline layer, the so-called polycrystalline-silicon/polysilicon (poly-Si). After PSG removal in wet-chemistry, ADE process can be performed to remove the wrap-around poly-Si layer.

As shown schematically in Figure 3, it is not only important to fully remove the poly-Si layer on the textured side, but also to isolate the edges to avoid the leakage current paths in a solar cell. We have observed that for both, as-deposited and annealed layers, the BSG layer acts as an excellent barrier layer against F_2, and thus an etch-stop. In fact, no measurable etching of BSG layer is observed even after applying the maximum F_2

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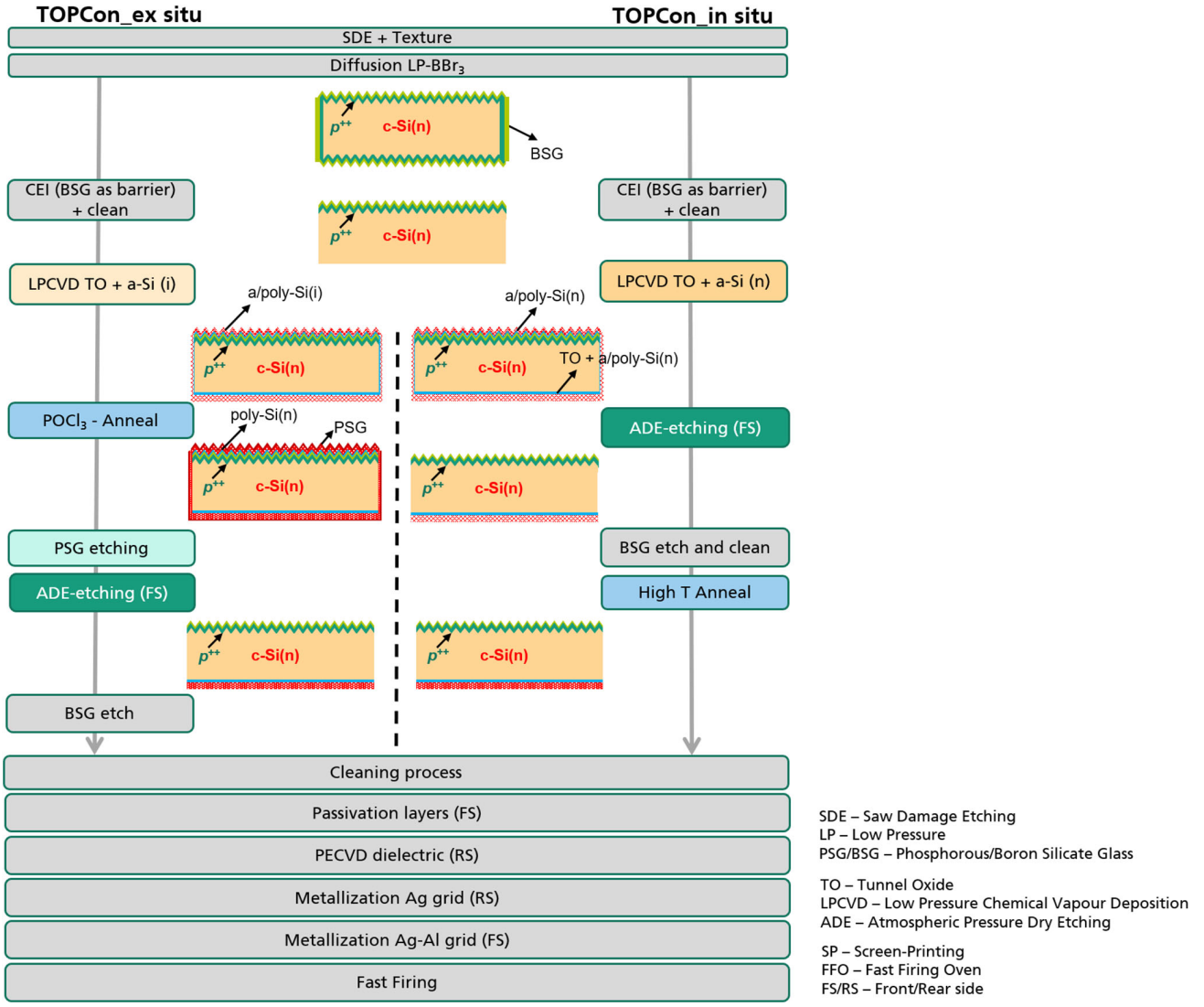

Figure 3. Process routes for both sides contacted n-TOPCon concepts using LPCVD polysilicon layers integrating ADE polysilicon etching process—TOPCon_ex situ featuring deposition of intrinsic LPCVD layers followed by ex situ doping in $POCl_3$ tube furnace, TOPCon_in situ featuring in situ phosphorous-doped LPCVD layers.

concentration possible in our setup (30%) to a substantially longer duration (>2.5 times) than the typical process time required to completely etch 180 nm poly-Si(n) layer. A high resistance of BSG layer against F_2 gas provides a wide process window while applying ADE for polysilicon etching. For ex situ route, ADE process is beneficial to perform after the $POCl_3$-anneal process rather than in as-deposited state, as performing the ADE process before ex situ doping leads to the following drawbacks: 1) higher chances for shunt formation due to diffusion of the phosphorous atoms through the BSG layer; 2) phosphorous doping of the edges that would require an additional subsequent SSE process for edge isolation.

For TOPCon_in situ, the deposition of phosphorus doped layers (a-Si(n)) is followed by ADE process for wrap-around removal of a-Si(n) layer on the textured-side, with a subsequent BSG etching and cleaning sequence. Afterward, a high-temperature annealing process is required to form poly-Si(n) layers at the rear.

For both routes, boron emitter passivation is then performed by depositing a passivation layer stack on the front side. In this work, the passivation is performed by first growing a thin low-temperature thermal oxide of 1–2 nm in a tube furnace before deposition of AlO_x/a-SiN_x:H using a PECVD tube furnace. PECVD a-SiN_x:H is then deposited on top of poly-Si(n) layer in the rear-side as a hydrogenation source. Afterward, metallization is performed by screen-printing Ag (rear) and Ag–Al (front) grids, followed by a fast-firing process.

2.4. Etching Progression

The progression of ADE etching process is studied in case of both predominantly amorphous layers in as-deposited state (relevant to the TOPCon_in situ route), and for polycrystalline layers formed after high-temperature annealing (relevant to the TOPCon_ex situ

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route). For these studies, we used cell-like precursors that are prepared using the process flow shown in Figure 3 till the ADE process step. ADE etching is performed for various process durations, keeping other parameters constant, to observe various stages of a-Si/poly-Si etching using high-resolution scanning beam electron microscopy (Zeiss Auriga 60). The results are summarized using **Figure 4** and **5** for ex situ doped annealed poly-Si(n) and in situ doped as-deposited a/poly-Si(n) layers, respectively.

In Figure 4, the SEM images clearly indicate that the etching of poly-Si layers preferentially starts on highly reactive sites such as defects/grain boundaries in the poly-Si layer. Indeed, the polycrystalline layers are known to comprise small grains of single crystals that are separated by thin grain boundaries consisting of extremely thin amorphous layer.[20] Depending upon deposition and annealing conditions, poly-Si layer is reported to have crystal grains that are either randomly distributed or have a columnar structure.[20,21] The cross-sectional image of the enhanced etch at boundary region (third image from left in Figure 4) indicates the columnar grain structure of poly-Si layer used in this work, with grain sizes in the range of 50–500 nm as estimated from the SEM images. A detailed estimation of the grain sizes is beyond the scope of this work.

Based upon the available literature on F_2 etching of silicon, preferential attack of F_2 on the reaction sites such as surface defects and grain boundaries is very likely to occur.[22,23] Once the etching leads to the opening of the grain boundaries, a larger surface area of poly-Si is exposed to the incoming F_2 species. Gradually, the crystal grains are etched in a preferential order, with the ERs

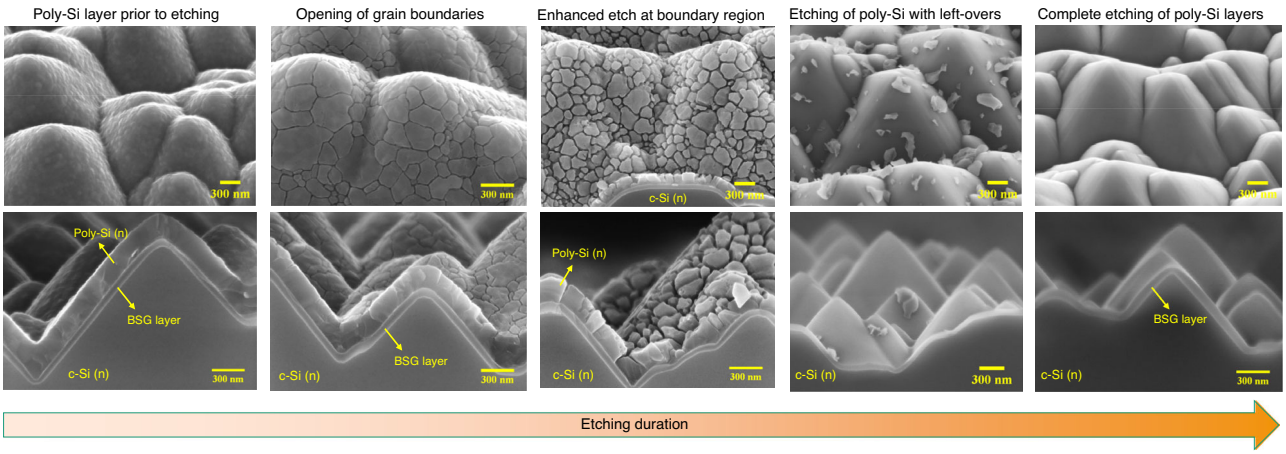

Figure 4. Tilted view (upper) and cross-sectional (lower) SEM images showing different phases of poly-Si etching after applying ADE process on n-doped polycrystalline silicon layers. Here, deposition of intrinsic a-Si layers is followed by ex situ doping in a $POCl_3$ tube furnace.

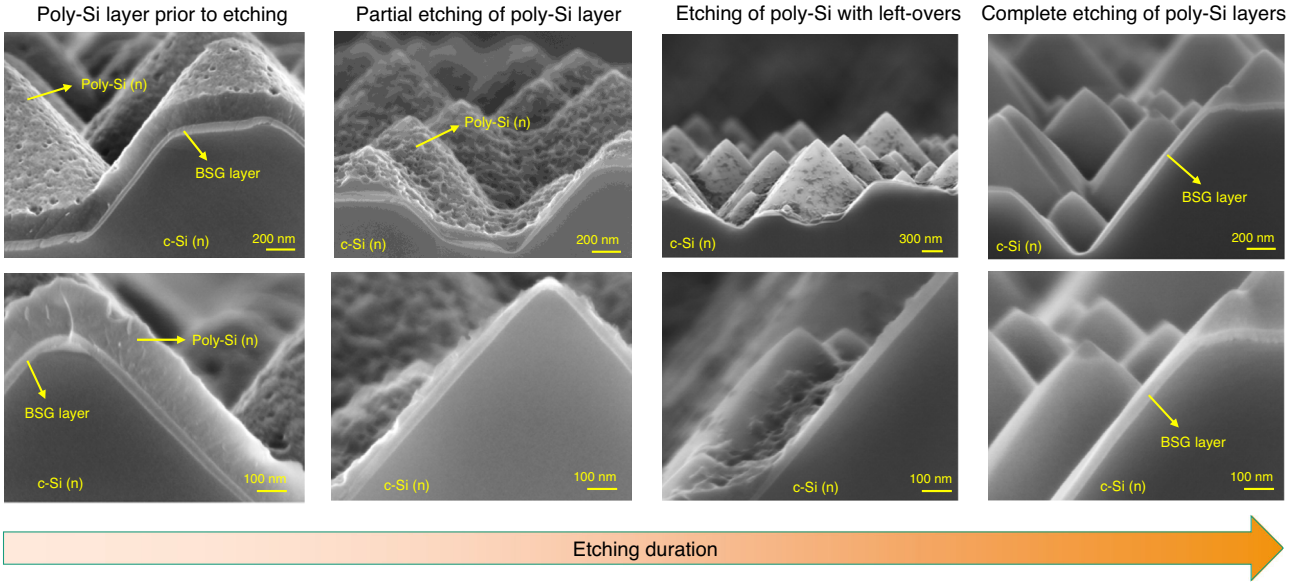

Figure 5. Tilted view (upper) and cross-sectional (lower) SEM images showing different phases of a/poly-Si etching after the exposure of in situ doped predominantly amorphous silicon layers to the F_2/N_2 gas mixture. The samples are not annealed after LPCVD deposition process.

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potentially decreasing with the increased packing of the atoms in the crystalline structure. Further investigations are required for the in-depth understanding of the etching mechanism. In Figure 5, it is observed that the etching progression for the as-deposited layers differs from the annealed layers in Figure 4.

For such predominantly amorphous layers, it is expected that the etching also starts preferentially on reaction sites such as surface defects and atomic steps, leading to the formation of the etch pits and the nanostructuring of the a-Si layer, before gradually etching it completely. Interestingly, it is observed that the pyramid valleys are the areas that are etched in the end.

3. Rear-Side Wrap-Around

Apart from etching of parasitic a-Si/poly-Si layer on the undesired side (front/textured side), the wafer edges also need to be etched to avoid the shunt paths in the solar cell. One way to avoid the leakage currents, especially for the reverse bias state, is to perform slight wrap-around etching of a-Si/poly-Si layer on the rear while etching the front side.

During ADE etching of the front side, the BSG layer acts as an excellent barrier; therefore, the etching process is self-limiting once the a-Si/poly-Si layer on front side is etched. However, it is important to not substantially over-etch the rear-side as it would then negatively impact the electrical performance and reverse-bias property of the solar cell. In addition, the rear-side Ag-grid must be designed to avoid printing on the cell area portions that are devoid of any a-Si/poly-Si layer. Therefore, the ADE etching needs to be optimized in such a way that the process results in the complete etching of a-Si/poly-Si layer in the front side, while enabling edge isolation and acceptable rear-side wrap-around.

Figure 6 shows the microscopically measured rear-side wrap-around for various ADE processes that differ in the F_2 concentration while keeping other parameters constant ($\nu = 28\ \mathrm{mm\ s^{-1}}$, $T_{\mathrm{wafer}} = 225\ ^{\circ}\mathrm{C}$).

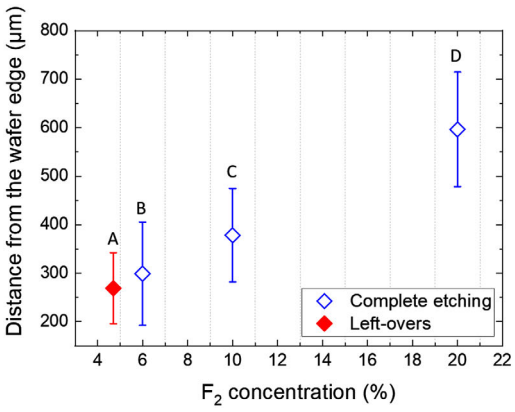
It is observed that for the constant process duration and temperature, an increasing F_2 concentration linearly increases the rear-side wrap-around distance. Although process A shows the lowest average wrap-around distance of 250 µm, the process is not able to yield complete etching of a-Si(n) on the front side, and thus not the ideal process. A slight increment in F_2 concentration to 6% yields a complete etching of a-Si(n) layer on the front side while at the same time also enabling a low average wrap-around distance of 300 µm. In contrast to this, a higher F_2 concentration leads to a further increment in the wrap-around distance. Nevertheless, the wrap-around distances shown here are still modest and are applicable in the solar cell manufacturing. For the sample with maximum F_2 concentration of 20%, SEM investigations of the rear-side wrap-around is performed, imaging the a-Si(n)/c-Si interface in every 500 µm distance from the wafer edge. The images are shown in **Figure 7**.

It is observed that the a-Si(n) layer is completely etched at the wafer edge. At 500 µm from the wafer edge, a thinner (40–50 µm) layer is found. At 1000 µm away from the wafer edge, no measurable thinning of a-Si(n) layer is observed although the images suggest slight roughening of the layer. The results suggest that, for the optimized ADE processes (example process B and C in Figure 6), a low rear-side wrap-around <500 µm can be expected.

4. Application in TOPCon Solar Cells

In **Figure 8**, photographs of solar cell precursors at different stages of solar cell production (TOPCon_in situ) are shown. It can be observed that the a-Si(n) layer on the textured side is completely removed after the ADE etching (Figure 8 (middle)), whereas the wrap-around of the rear-side (Figure 8 (right)) is maintained to be very small and is hard to notice visually.

First cell results achieved after integrating ADE process in both ex situ (TOPCon_ex situ) and in situ (TOPCon_in situ) processing routes, as shown in Figure 3, are show in **Figure 9**. Note that the ex situ and in situ cell results are not directly comparable as the



Sample ID	F_2 concn. (%)	Etching results (front-side)
A	4.7	Traces left
B	6	Complete
C	10	Complete
D	20	Complete

Figure 6. (Left) Plot showing rear-side wrap-around (average and standard deviation of 20 points) measured using confocal microscope for ADE processes, and (right) Table showing the respective process information. Here, deposition of 180 nm in situ doped a-Si(n) by LPCVD is followed by ADE etching. F_2 concentration is varied by changing gas flux ratios (F_2/N_2 and N_2) and total gas flux, whereas all other parameters (T_{wafer}, ν) are kept constant. The red full diamond represents a process where a-Si(n) leftovers are identified on the front-side after ADE, whereas the blue empty diamond represents processes leading to complete etching of a-Si(n) layer on the front-side.

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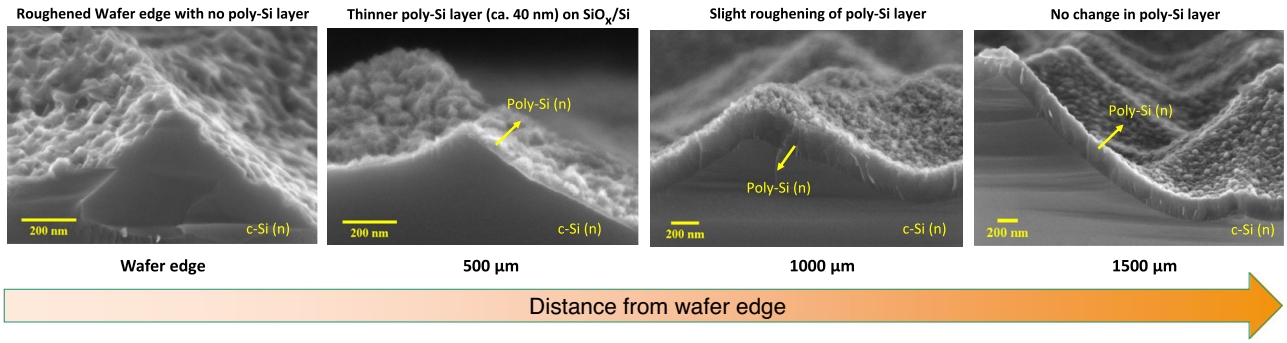

Figure 7. SEM images showing presence/absence of a-Si(n) layer for an increasing distance from the wafer-edge for the process D in Figure 6.

Figure 8. Photographs of solar cell precursors showing: (left) textured side after LPCVD deposition of a-Si(n) on top of BSG layer (left), (middle) textured side after ADE etching of a-Si(n) layer, and (right) rear side after ADE etching of a-Si(n) layer on the textured side.

samples have been processed in different batches at different times, partly received different processing recipes in various process steps.

The solar cells from these batches reach highest conversion efficiency (η) of 21.60% for TOPCon_ex situ and 21.95% for TOPCon_in situ routes, respectively. The cells from these batches are mainly limited by lower-than-expected FF and V_{OC} values. The optimization of these parameters is ongoing in current batches, by mainly looking to improve the passivation and metallization-related process steps. Meanwhile, for the evaluation of the single-sided etching of a-Si/poly-Si, parallel resistance (S_{shunt}) is the important parameter to consider. Both batches showed excellent values of shunt resistance ($S_{shunt,avg.} > 1500\,k\Omega\,cm^2$), which underlines complete removal of parasitic a-Si/poly-Si layers by the ADE process. Furthermore, high pseudo-fill factor (pFF) values also suggest no influence of shunt resistance on FF values. In **Figure 10** (left), reverse current density (J_{rev}) measurement of solar cells performed at the reverse bias of $-12\,V$ are plotted for both TOPCon_ex situ and TOPCon_in situ routes. In both cases, ADE processing enables low reverse current density ($J_{rev,avg} < 0.8\,mA\,cm^{-2}$) values, with no hotspots observed in thermography measurements. A representative infrared image of the fabricated TOPCon solar cell is shown in Figure 10 (right). In summary, cell results for both routes prove the effectiveness of the single-sided a-Si/poly-Si etching process developed in this work.

Very recently, the conversion efficiency of large area TOPCon solar cells ($A_{cell} = 244.51\,cm^2$) with in situ phosphorous doped LPCVD polysilicon and applying ADE etching for wrap-around removal has been increased to 23.3% with following electrical parameters: $V_{OC} = 702.7\,mV$, $J_{SC} = 40.1\,mA\,cm^{-2}$, FF = 81.3%, $\eta = 23.3\%$, independently certified by Fraunhofer ISE CalLab PV Cells. The optimizations performed in the process sequence to achieve this are beyond the scope of this article and will be discussed in future publications.

5. Conclusion

In this work, we present ADE to perform single-sided etching of amorphous/polycrystalline silicon (a-Si/poly-Si) layers to fabricate industrial-type TOPCon solar cells on n-type substrates. The etching process has been developed for LPCVD-deposited phosphorous-doped polysilicon layers either in as-deposited state or after the annealing step. High etching rates of $>3\,\mu m\,min^{-1}$ are achieved for a-Si/poly-Si layers in SDE surface at a low F_2 concentration of 10% and $T_{wafer} = 225\,^{\circ}C$. On textured cell-like processors, the currently applied process leads to an etching rate of 1.5–4.5 $\mu m\,min^{-1}$, depending upon the applied process conditions. This means a typical a-Si/poly-Si layer thickness of 200 nm on large (M2) wafer size is completely etched within ≈3–6 s while maintaining excellent single-sidedness. Further increment in ER can be achieved by increasing the process temperature, the fluorine concentration, the fluorine flux, and enlarging the reactor size. Nevertheless, already the current process offers the highest etching rates in comparison with the other alternatives that are reported in the literature so far. The ADE process tool used in this work enables automated load/unload and inline transport of the wafer substrates, which underscores its applicability in high-throughput manufacturing scenario.

ADE shows extremely high selectivity of silicon layers to the borosilicate glass (BSG) layer, which is typically formed during boron emitter diffusion step and can therefore be used as a perfectly stable etch-stop for F_2 etching. The ADE process also shows an excellent edge isolation property while limiting the wrap-around of the rear-side to <500 µm. With considerations on the reverse-bias behavior of the cell and ensuring a lean process flow, we propose to implement ADE after $POCl_3$ annealing for ex situ doped layers, whereas in as-deposited state for the in situ doped layers. First TOPCon solar cells using ex situ and in situ doped poly-Si layers reach a maximum conversion efficiency of 21.6% and 21.95%, respectively. The cells presented in this work are mainly limited by a lower V_{OC} and FF; nevertheless, the cells show excellent parallel resistance ($S_{shunt,avg.} > 1500\,k\Omega\,cm^2$) and

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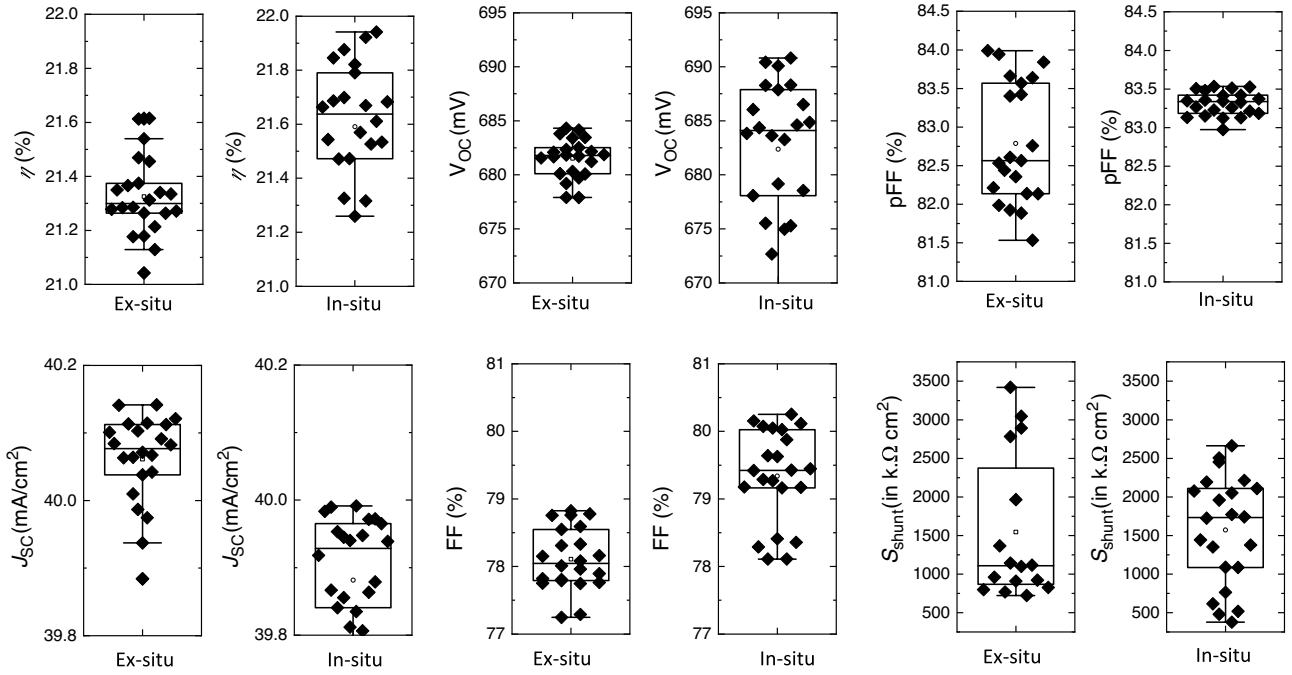

Figure 9. Current-voltage (I–V) results of the first-generation bifacial TOPCon cells ($A_{cell} = 15.6 \times 15.6\ cm^2$) incorporating ADE poly-Si etching process for both ex situ (TOPCon_ex situ) and in situ (TOPCon_in situ) process routes.

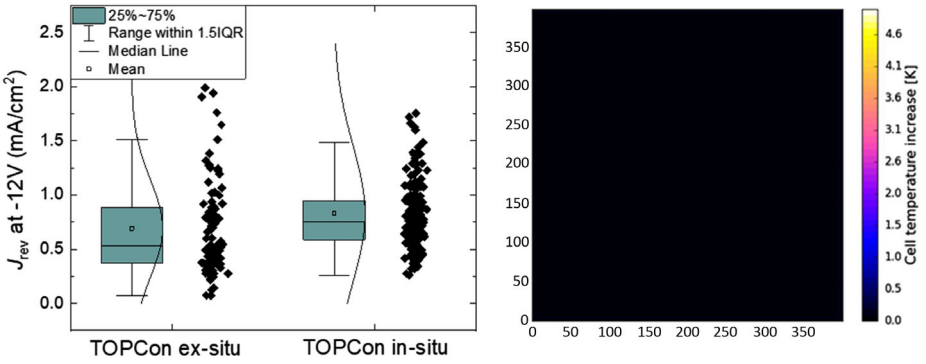

Figure 10. (Left) Reverse current density (J_{rev}) measured by applying a reverse bias voltage of −12 V for both ex situ and in situ routes; (right) infrared image of a representative TOPCon solar cell using thermography that shows no formation of hot-spots in the whole cell area.

high pFF values, confirming a successful transfer of the ADE process to the TOPCon solar cell processing. The process improvements have recently improved the electrical performance of TOPCon cells featuring in situ doped layer and ADE wrap-around removal with an independently certified conversion efficiency of 23.3%, featuring $V_{OC} > 700$ mV. In addition, for several batches processed already in our pilot line, ADE process consistently shows reproducible results of low reverse current density ($J_{rev,avg} < 0.8\ mA\ cm^{-2}$) measured at the bias potential of −12 V, with no hotspots observed in thermography measurements. Although the current study is performed based upon current state-of-the-art LPCVD-deposited a-Si/poly-Si layers, the results are also applicable to alternative a-Si/poly-Si layer deposited by other technologies such as PECVD and APCVD. In fact, we have observed that the wrap-around of PECVD-deposited a-Si/poly-Si layers is etched even faster due to a lower wrap-around thickness in comparison with the LPCVD-deposited layers. The process developed in our prototype tool is swiftly transferable to the currently offered high-throughput version of the industrial tool,[24] thus making ADE etching highly relevant for the PV industry. Last but not least, the use of F_2 gas with zero global warming potential (GWP) and an easy abatement of waste products using existing wet scrubber systems help toward lowering the environmental footprint of PV production plants.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Keywords

etching, passivated contacts, polysilicon, reverse-current density, solar cells, TOPCon

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