Received: 21 June 2021 | Revised: 10 September 2021 | Accepted: 29 September 2021

DOI: 10.1002/pip.3491

RESEARCH ARTICLE

PROGRESS IN PHOTOVOLTAICS WILEY

Optimized front TCO and metal grid electrode for module-integrated perovskite–silicon tandem solar cells

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Funding information
Deutsche Bundesstiftung Umwelt

Abstract

To unlock the full potential of perovskite–silicon tandem solar cells with >30% efficiency at presumably low cost, the transparent conductive oxides (TCOs) and metal grid at the front side need to be adapted compared to classical silicon heterojunction (SHJ) solar cells. By means of optical and electrical modelling, we consider the main aspects to optimize the front electrode for the tandem case, where in contrast to silicon single junction devices, there are (i) different optical properties including a lower refractive index of the perovskite absorber (ii) about half the current, thus quarter the resistive power losses for the same series resistance contribution (iii) lateral transport at the front needs to be provided solely by the front TCO layer and (iv) lower thermal stability of the perovskite, which affects TCO deposition conditions and results in a less efficient sintering of the silver screen printing pastes. This study concludes that compared to silicon heterojunction cells, the thickness of the front TCO should be reduced from 75 nm to around 20 nm, resulting in less parasitic absorption and a potential cost reduction of 1.46 €ct/cell for ITO. We investigate the impact of different front metallization including plating and silver screen printing and showcase that for multi-wire interconnection concepts, the number of wires can be reduced from 18 wires to 9 or even less depending on the front metallization. Finally, we give an outlook on the silver consumption and levelized cost of electricity.

KEYWORDS
cost analysis, perovskite–silicon tandem solar cells, photovoltaics, Sentaurus TCAD, simulation

1 | INTRODUCTION

Perovskite–silicon tandem solar cells have proven their efficiency potential at laboratory scale[1,2] by exceeding the silicon single junction limit and are expected to further decrease the costs of electricity[3,4] which is crucial to compete with the established Si PV technologies. However, many upscaling aspects are still in their infancy, for example, how the layer stack of the perovskite top cell will look like and which deposition technologies will be used. In any case a front electrode, that is, a transparent conductive oxide (TCO) and metal grid, is further needed. The conversion efficiency of monolithic two-terminal tandem devices has a higher tolerance

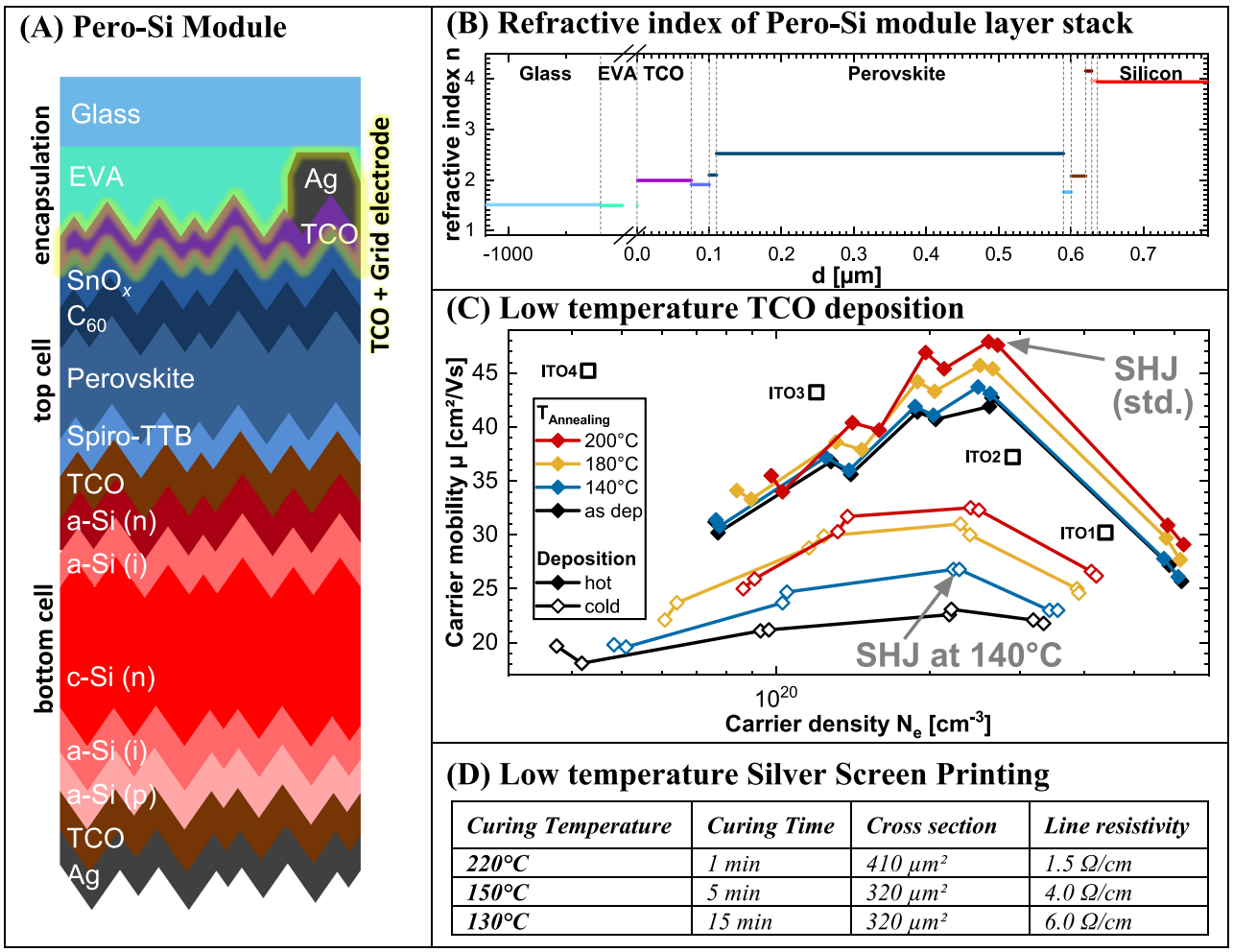
to series resistances compared to single junction devices like for example the silicon heterojunction (SHJ) technology, since only about half the current density is collected by the electrodes. Thus, for a given series resistance contribution of the front electrode, only a quarter of the resistive power loss is to be expected. However, using perovskite as a top cell absorber also has impact on the following:

(i) **Optical properties:** Most perovskites feature a refractive index of around $n = 2.5$, compared to silicon with n around 4. This changes the requirements on the TCO layer with respect to its function as an anti-reflection coating (ARC), compared to SHJ cells.

(ii) **Lateral transport:** The thin perovskite absorber is expected to provide almost no lateral conductivity towards the metal grid unlike SHJ devices where the lateral current transport of the silicon bulk can be significant.[5,6]

(iii) **Thermal stability:** The thermal device stability and hence the temperature for back-end processing is reduced to around 100–130°C due to the perovskite, whereas it is typically around 220°C for SHJ solar cells. Therefore, ultra-low-temperature TCO processing and metallization is needed. However, the lower limit for the deposition and annealing temperature of the TCO and the sintering temperature of the silver screen-printing (Ag SP) pastes affects the material properties which leads to a possible increase of the TCO sheet resistance and the line resistivities of the screen-printed silver fingers.

Based on the expertise and learning of recent years of the SHJ baseline processes, this work elaborates on how the front TCO and grid



Curing Temperature	*Curing Time*	*Cross section*	*Line resistivity*
220°C	*1 min*	*410 µm²*	*1.5 Ω/cm*
150°C	*5 min*	*320 µm²*	*4.0 Ω/cm*
130°C	*15 min*	*320 µm²*	*6.0 Ω/cm*

FIGURE 1 (A) The investigated perovskite–silicon tandem module featuring the highlighted front TCO and grid electrode at the top cell front side. (B) the refractive index n at 600 nm for the layer stack of the perovskite–silicon tandem module. (C) Measured mobility µ and carrier density N_e of the front TCO for the SHJ baseline process with standard conditions ('SHJ std.' at 200°C) and for lower deposition and annealing temperatures ('SHJ at 140°C'). 'ITO1'–'ITO4' show measured data of a more suitable low-temperature TCO deposition which is used for the simulations. (D) Silver screen printing (Ag SP) parameters for a low-temperature paste at two curing temperatures (130°C and 150°C) and a standard SHJ paste (220°C with higher aspect ratio). The values are based on experimental data and show an estimate for feasible SP processes at 35-µm finger width. The line resistivity ρ_{line} and cross-sections are used as input for the device simulation and cost calculation [Colour figure can be viewed at wileyonlinelibrary.com]

electrode should be adapted for perovskite–silicon tandem solar cells within a module. Section 2 will introduce the experimental background and modelling approach, which is used in the following to optimize the TCO electrode in Section 3. Moving on with the optimized TCO electrode, we investigate the finger metallization and interconnection concept (Section 4) and its implications on the costs (Section 5).

2 | EXPERIMENTAL BACKGROUND AND MODELLING APPROACH

The optical simulation model is set up in Sentaurus TCAD[7] based on the perovskite–silicon tandem cell published by Schulze et al.[8] featuring a monolithic p-i-n perovskite top cell and a textured SHJ bottom cell. The optical model was experimentally validated in[9] where also a roadmap towards higher optical performance and current matching was proposed including a higher perovskite absorber thickness of 480 nm, thinner TCO recombination layer of 20 nm and a both-side textured cell.

Figure 1A shows the perovskite–silicon (Pero-Si) tandem cell as used in this work with textured bottom cell including glass and encapsulant (EVA for simplicity reasons) as used in a module. The investigated front TCO and grid electrode is highlighted. The optical data of the front TCO (i.e., ITO) originates from in-house measurements at Fraunhofer ISE including a variation of different oxygen flows (O_2 flow from 0.0 to 0.7 sccm, labelled as 'ITO1' to 'ITO4').[10] Detailed simulation models and parameters including the thicknesses and the used complex refractive indices for each layer can be found in Table 1. Figure 1B shows the refractive index n (at 600 nm) of all thin layers of the investigated perovskite–silicon tandem layer stack of Figure 1A. One can see that the TCO is stacked between the EVA ($n = 1.5$) and the thin ETL layers adjacent to the perovskite with a refractive index of around $n = 2.5$ which changes the optical requirements of the TCO layer compared to a silicon single junction module ($n_{cSi} = 4$). From the model, we obtain the parasitic absorption in each thin layer including the front TCO and the generated current density in both the perovskite and silicon absorbers. Current-matching of the two sub cells has been done accurately for one single case by adaption of the perovskite bandgap and absorber thickness. For all other cases, the short-circuit current of the tandem device was current-matched by $j_{sc,matched} = 0.5 \cdot (j_{sc,Pero} + j_{sc,Si})$ for reasons of simplicity. Since the current mismatch $j_{sc,Pero} - j_{sc,Si}$ of the two sub cells lies between -0.5 and 0.5 mA/cm^2 for the textured case, this is a good approximation and could easily performed for all cases by small bandgap adaptions of the perovskite and/or slightly varied absorber thicknesses.

For the electrical simulation, we use input parameters based on measurements of low-temperature deposited TCO and silver screen printed metal fingers as discussed in the following. Figure 1C shows the TCO mobility μ as a function of the carrier density N_e (i.e., different oxygen flows) for hot (filled symbols) and cold (open symbols) deposition, as well as different annealing temperatures. The TCO deposited with the SHJ baseline process (symbols connected by lines, deposition temperature ~200°C) shows good mobilities up to around 48 cm^2/Vs after annealing at 200°C (shown in red). This baseline process uses high quality poly-crystalline films based on an ITO target which is ideal for application on SHJ with deposition temperatures around 200°C. When simply reducing the temperatures to 140°C and cold deposition (shown in blue, open symbols), the carrier mobility is reduced to ~27 cm^2/Vs while the carrier density is not affected which results in higher sheet resistances of the TCO and thus additional resistive power losses. Therefore, a different, more suitable ultra-low-temperature TCO deposition process is needed for the Pero-Si tandem device. Figure 1C additionally shows experimental data of another low temperature TCO deposition process, which is denoted from 'ITO1' to 'ITO4'. Here, a different ITO composition with higher SnO_2 doping was used to increase the conductivity of the amorphous films, which demonstrates that higher carrier mobilities can also be achieved for low temperature processed TCOs. We use 'ITO1' to 'ITO4' (both electrical and optical properties taken from measurements) as simulation input for the front TCO of the tandem device.

TABLE 1 Optical simulation parameters

Quantity	Value
Sentaurus TCAD[7]	
Version	Q-2019.12
Global	
Temperature	298.15 K
Spectrum	AM1.5 g, 1 sun (from PV Lighthouse[11])
Layer stack	
Encapsulation	1-mm glass,[12] 200-µm EVA,[12]
ITO (i.e., TCO) layers	varied (O_2 flow and thickness), complex refractive index from in-house measurements at Fraunhofer ISE
Perovskite top cell	25-nm SnO_x, Fraunhofer IST, 10-nm C_{60}, Fraunhofer IST, 480-nm perovskite,[13,14] 11-nm PTAA, Fraunhofer IST
Interconnection layers	20 nm ReCO (ITO), IST SiT, Schinke et al.[15] extended with FCA model of Baker-Finch[16] (same for all poly-Si layers)
SHJ front	8-nm a-Si(n)[17] 8-nm a-Si(i)[17]
Silicon bottom cell	180 µm, 1 Ω cm (n-type), Schinke et al.[15] extended with FCA model of Baker-Finch[16]
SHJ rear + metallization	8-nm a-Si(i)[17] 15-nm a-Si(p),[17] 70-nm ITO (lowly doped for monofacial application, Fraunhofer IST), silver[18] (textured rear side)
Modelling	
Raytracing	In all thick layers, i.e., glass, EVA and silicon
Transfer-matrix method (TMM)	In all thin-film layers including the front TCO and perovskite absorber
Phong	To account for the rough morphology of the perovskite top cell improving the light trapping properties of the silicon absorber

Furthermore, the influence of the lower temperature stability on the screen-printed silver contacts must be considered. Figure 1D shows the silver screen-printing (Ag SP) parameters for a low-temperature paste at two curing temperatures (130°C and 150°C) and a standard SHJ paste (220°C with higher aspect ratio, i.e., finger height). The values are based on experimental data and show an estimate for feasible SP processes at 35-µm geometrical finger width. We experimentally observe a significant increase in line resistivity ρ_{line} for the Ag fingers from around 1.5 Ω/cm to 4–6 Ω/cm when using ultra-low-temperature Ag SP pastes instead of the SHJ baseline SP process. The improvement of the line resistivity for higher annealing temperatures is due to the sintering of the Ag paste.[19] Figure 1D is used as input for the device simulation and cost calculation.

The electrical simulation yields a series resistance contribution of the front electrode $R_S^{front} = R_S^{lateral} + R_S^{finger} + R_S^{wires}$, where $R_S^{lateral}$ denotes the lateral series resistance arising from front TCO and top cell; and R_S^{finger} denotes the series resistance due to the metal fingers, which are both obtained using Quokka3.[20] The series resistance of the multi-wire interconnection R_S^{wires} is calculated according to Witteck et al.[21] and Goetzberger et al.[22] assuming copper wires with a diameter of 350 µm.[23] Subsequently, we calculate the internal power $P_{int} = V_{mpp,int} \cdot j_{mpp}$ of the Pero-Si tandem device, which does not include the electrical losses of the front TCO and grid electrode, but which incorporates the parasitic absorption losses of the optical TCAD model (especially of the front TCO) and includes shading losses of the metal fingers and multi-wires (with optical width of 210 µm due to back reflection of the round wires according to Witteck et al.[21] The j_{mpp} is based on the assumptions according to Messmer et al.[9] using the optical generation current from the TCAD model. For the internal voltage at MPP, we assume a constant value of $V_{mpp,int} = 1.6$ V, of which we attribute 960 mV to the perovskite top cell (with the improved electrical properties according to Schulze et al.[8]) and 642 mV to the SHJ bottom cell (at half a sun!). Please note that in a real device, a decreased device current also slightly decreases $V_{mpp,int}$ which is not considered here and leads to a slight overestimate of low efficiency devices. Subsequently, the output power P_{out} of the tandem device is calculated by

$$P_{out} = P_{int} - P_{R_S}^{front} = \left[V_{mpp,int} \cdot j_{mpp}\right] - \left[R_S^{front} \cdot {j_{mpp}}^2\right] \quad (1)$$

We assume the contact resistivities of the ETL/TCO interface and the TCO/metal interface to be negligible (1 mΩ/cm^2) unless stated otherwise and perform a separate sensitivity analysis in Section 3.2.

3 | OPTIMIZATIION OF THE FRONT TCO ELECTRODE

3.1 | Analysis of optical losses

In a first step, the front TCO electrode is optimized. For this, we investigated four different ITO (In_2O_3/SnO_2: 90/10 wt.%) layers ('ITO1' to 'ITO4', see Table 2) deposited under varying oxygen flows whereby the complex refractive indices are obtained via spectroscopic ellipsometry. The optical simulations of the complete layer stack of Figure 1A are carried out with varied TCO thickness.

Figure 2A shows the resulting reflection and absorption currents as a function of the front TCO thickness from 75 to 5 nm for the whole Pero-Si Module with planar cell front for a TCO with low O_2 content ('ITO1', Figure 1C). One can see that the reflection (shown in green) is relatively high with an equivalent current loss of more than 5 mA/cm^2. This is due to the reflection at the planar air/glass interface (about 3 mA/cm^2) and additional reflection at the planar cell front side where reflection peaks occur (not shown) for different wavelengths depending on the TCO thickness. The parasitic absorption in the encapsulation, the front layers, the front TCO, rear layers and the rear metal are also shown in Figure 2 (see legend). One can see that the parasitic absorption in the front TCO (dark blue) is very high for a thickness of 75 nm (about 3.5 mA/cm^2) which is significantly reduced by thinning the TCO down to 5 nm. This leads to an increased current generation (shown in red) within

TABLE 2 Electrical simulation parameters

Quantity	Value
Quokka3[20]	
Version	1.2.8
Wafer size	M6 format (166 × 166 mm^2)
Physical finger width	35 µm
Optical finger width	50% of physical finger width[21,24]
Wire diameter	350 µm
Optical width of wires	210 µm (factor 0.6[21])
Front TCOs[10]	
ITO 1 (O_2 flow: 0.0 sccm)	$N_e = 4.4{\cdot}10^{20}$ cm^{-3}, $\mu_e = 30.2$ cm^2/Vs $R_{sheet}(d = 75\text{ nm}) = 63$ Ω/sq
ITO 2 (O_2 flow: 0.3 sccm)	$N_e = 2.9{\cdot}10^{20}$ cm^{-3}, $\mu_e = 37.2$ cm^2/Vs $R_{sheet}(d = 75\text{ nm}) = 77$ Ω/sq
ITO 3 (O_2 flow: 0.5 sccm)	$N_e = 1.2{\cdot}10^{20}$ cm^{-3}, $\mu_e = 43.2$ cm^2/Vs $R_{sheet}(d = 75\text{ nm}) = 155$ Ω/sq
ITO 4 (O_2 flow: 0.7 sccm)	$N_e = 4.3{\cdot}10^{19}$ cm^{-3}, $\mu_e = 45.2$ cm^2/Vs $R_{sheet}(d = 75\text{ nm}) = 427$ Ω/sq
SHJ reference	
Silicon bulk	180 µm thick, 1 Ωcm n-type, $\tau = 12$ ms
V_{oc}	740 mV at 1 sun
Others	
Contact resistivities at TCO/ETL	1 mΩ cm^2 (assumed negligibly small)
Contact resistivities at TCO/Ag	1 mΩ cm^2 (assumed negligibly small)

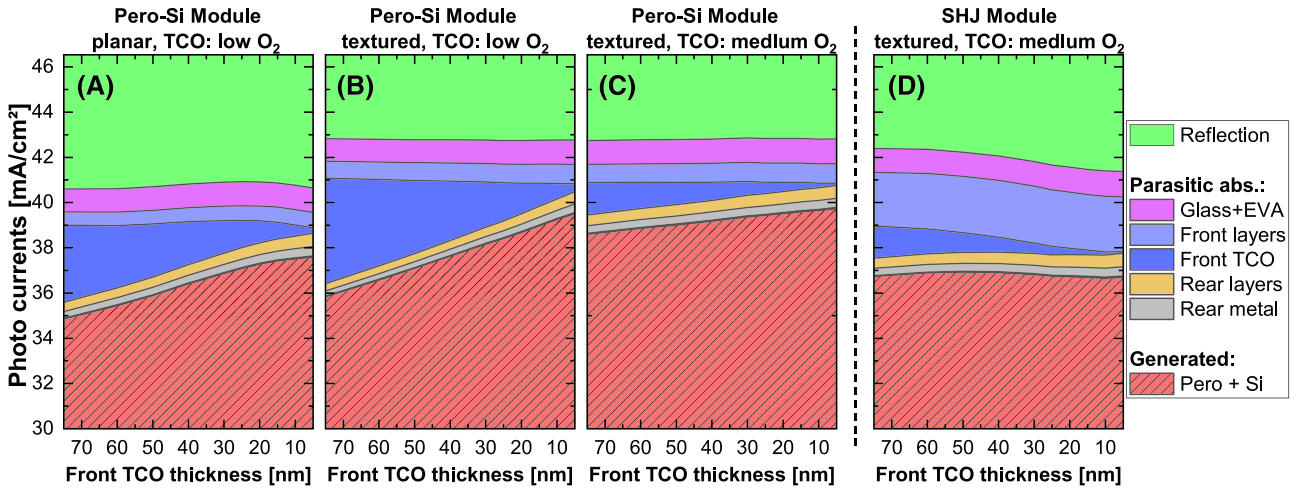


FIGURE 2 Optical currents of the simulated Pero-Si module for (A) a planar cell front side with a TCO featuring a low oxygen content ('ITO1', see Table 2), (B) a textured cell front side with the same ITO and (C) textured cell front side with a more transparent TCO ('ITO3'). (D) Comparison to a SHJ module, where the reduction of the TCO thickness leads to higher reflection losses due to its anti-reflection coating (ARC) properties [Colour figure can be viewed at wileyonlinelibrary.com]

the perovskite and silicon absorber. About 2.5 mA/cm^2 can be gained by the thickness reduction.

When moving to a textured cell (Figure 2B), we see that the reflection is significantly reduced to 3.5 mA/cm^2. The remaining reflection is mostly due to the planar air/glass interface which does not feature any ARC. However, due to textured cell front side, the optical path length through the front layers is increased leading to an increase in parasitic absorption, especially in the front TCO. This makes the reduction of the TCO thickness even more effective.

In Figure 2C, the photon currents for the same Pero-Si Module with textured cell front is displayed when using a higher oxygen content, i.e. lower doping and thus a lower carrier concentration, for the front TCO ('ITO3', Figure 1C). The parasitic absorption is much lower due to the higher infrared transparency of the TCO. Still, one can see that the reduction of the TCO thickness leads to a higher generated current in the perovskite and the silicon absorber. This contrasts with an SHJ module as shown in Figure 2D, where the TCO serves as an ARC. In this case, the TCO thickness reduction leads to an increase in reflection which counterbalances the reduction of the parasitic TCO absorption leading to a generated current in the silicon absorber (shown in red) that is almost unchanged. Without glass and EVA, the degraded anti-reflection properties for thinner TCO layers would have an even greater impact on reduced current generation in SHJ single junction cells (not shown).

One can conclude in terms of optical properties that a reduced front TCO thickness is beneficial for the perovskite–silicon tandem module since the parasitic absorption is minimized while maintaining low reflection. (Moreover, using SunSolve,[25] we see that the aesthetics of the module is maintained showing a nearly black module appearance.) However, this thickness reduction is counterbalanced by the electrical properties which will be investigated in the next subsection.

3.2 | Analysis of electrical losses

The electrical losses of the front TCO (here ITO) are analysed in Figure 3 for a textured device. One can see the internal power P_{int} according to Equation 1 (Figure 3A, grey diamonds) as a function of the ITO thickness (varied from 75 to 10 nm), the ITO oxygen flow (increasing O_2 content from 'ITO1' to 'ITO4') and front finger pitch (varied from 1 to 2.5 mm within each segment). P_{int} lumps the optical effects of the transparency of the ITO and the shading of the front metallization (where the optical finger width is 50% of the geometrical finger width in the module).[21,24] Therefore, P_{int} is increased from left to right for using more transparent and thinner ITOs and increased front finger pitch, i.e. less fingers. On the other hand, these optical gains are linked to an increased series resistance: The contribution from the front metal finger R_S^{finger} (shown as grey bars, see right axis) increases with larger finger pitch due to less fingers per cell. $R_S^{lateral}$ is equal to R_S^{ITO} here, since the perovskite top cell typically has a much higher sheet resistance with respect to the ITO due to its lower carrier mobility and concentration.[26,27] Unlike for SHJ cells, this confines lateral transport in the TCO and prevents efficient utilization of the absorber for lateral transport.[5,6] One can see that $R_S^{lateral}$ (light grey bars, right y-axis) is increased for higher oxygen content (i.e., higher sheet resistances) of the ITO and higher finger pitches due to longer transport length through the ITO layer. The series resistance contribution from the wires R_S^{wire} is shown in dark grey and is calculated for an M6 wafer (full square, 166 × 166 mm^2) with multi-wire interconnection (nine wires) and Ag screen printed metallization (finger width = 35 µm and line resistivity of 1.5 Ω/cm, which was chosen here despite the current technological limitations to focus on the TCO optimization and make it comparable to Figure 3B).

Consequently, we get a trade-off between the optical and electrical properties of the TCO which leads to the output power P_{out} of the

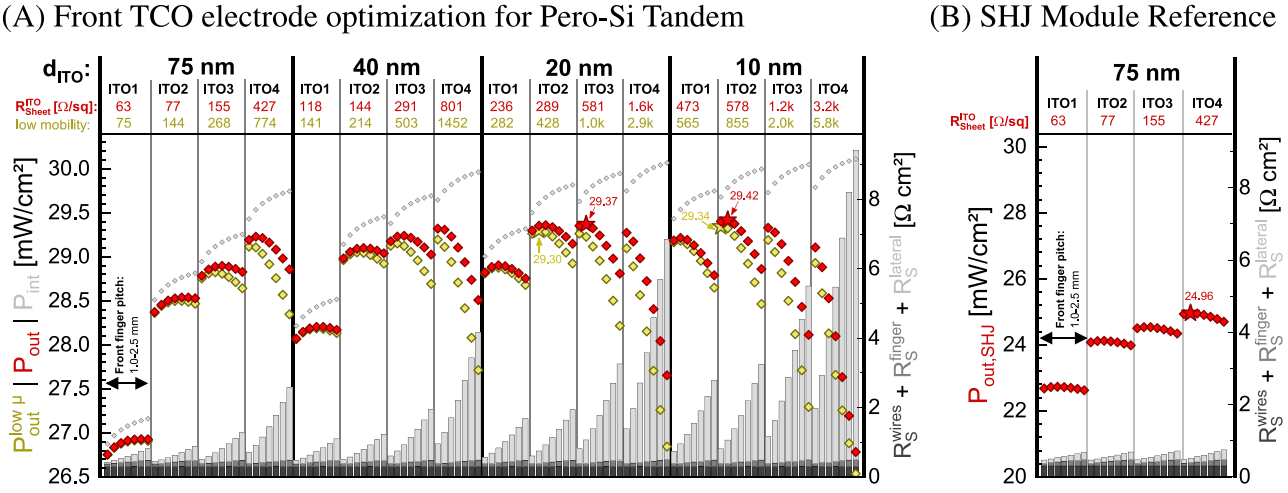


FIGURE 3 Optimization of the front TCO electrode: (A) tandem output power P_{out} for high (low) mobility TCO (here ITO) in red (yellow). The right axis shows the series resistance of the metal grid (dark grey) and lateral resistance within TCO (light grey). The TCO thickness d_{ITO}, TCO sheet resistance (ITO1–ITO4) as well as the metal finger pitch is optimized (see star). (B) the SHJ module as a reference with 75-nm ITO, where the lateral R_S is much smaller due to lateral conductance of the silicon absorber. To be comparable, both parts (A) and (B) are for a M6 wafer with 9 wire interconnection [Colour figure can be viewed at wileyonlinelibrary.com]

Pero-Si module according to Equation 1. P_{out} is shown in Figure 3A (in red) for 'ITO1' to 'ITO4' as introduced in Section 2. One can see that the power output is maximized at 29.42 mW/cm^2 by reducing the ITO thickness from 75 to 10 nm, using 'ITO2' and a finger pitch of 1.25 mm (see red star). However, due to technological feasibility a thicker ITO layer may be required: When using 20 nm of 'ITO3', the power output is still almost equally high (29.37 mW/cm^2, red star). Alternatively, also 'ITO2' with a higher finger pitch of 1.5 mm achieves similar power outputs.

Figure 3A additionally shows the impact of a low-mobility TCO (yellow diamonds), where we assume an only moderate carrier mobility of 25 cm^2/Vs for the 'ITO1' to 'ITO4'. This could showcase the additional power losses when for example using the non-ideal ITO deposition of a SHJ baseline process as introduced in Figure 1C ('SHJ cold') or when using other TCOs with typically feature lower mobilities (e.g., aluminium-doped zinc oxide, i.e., AZO[28]). The additional power losses are expected especially for thinner and more transparent TCO properties, but still, in our case, the power output is maximized for a thickness of 10 to 20 nm at slightly lower finger pitches.

Finally, we compare these findings to a standard SHJ module featuring a 75 nm thick ITO (see Figure 3B). First of all, we see that $P_{out,SHJ}$ is maximized for the most transparent TCO ('ITO4') and a finger pitch of 1.25 mm (see red star in Figure 3B), as it is also the case for the Pero-Si module with same TCO thickness of 75 nm (Figure 3A, left). However, for finger pitches above the optimum pitch, we see that the output power $P_{out,SHJ}$ for the SHJ does not drop as quickly as for the Pero-Si tandem device. The respective power loss originates from $R_S^{lateral}$ which is much lower for the SHJ module (see light grey bars in Figure 3B) than for the Pero-Si device using the same TCO properties (light grey bars in Figure 3A, left) despite the about two time higher current. The reason for $R_S^{lateral}$ being much smaller in the SHJ case lies in the silicon bulk which provides a parallel path for the lateral current transport besides the TCO.[5,6] For the Pero-Si tandem, the lateral current transport towards the metal contacts must be almost fully provided by the TCO which leads to a comparably high power loss for increased TCO sheet resistances and finger pitches. Since we used the same wafer size, finger metallization and interconnection for this SHJ module, R_S^{finger} and R_S^{wires} remain the same as for the Pero-Si module. For this comparison, we used the same high carrier lifetime ($\tau = 12$ ms) and good passivation quality ($V_{oc,1\ sun} = 740$ mV) for the bottom cell of the Pero-Si and the SHJ simulation.

The contact resistivities at the full ETL/TCO interface and the TCO/metal contact are assumed to be both negligible (1 mΩ cm^2) and the dependence on the TCO doping concentration, as observed, for example, for SHJ[29] is neglected. To see the influence of the contact resistivities, we performed a sensitivity analysis: For 10 times the TCO/metal contact resistivity the R_S^{front} is increased by 0.2 to 0.4 Ω cm^2 (depending on the finger pitch/contact fraction), and for 100 times the ETL/TCO contact resistivity, the R_S^{front} is increased by 0.1 Ω cm^2 (which is a simple linear dependence given the full-area nature of the ohmic contact).

4 | FINGER METALLIZATION AND INTERCONNECTION CONCEPT

Moving on with an ITO thickness of 20 nm, we investigate the influence of the finger metallization and the interconnection concept. All simulations are performed on an M6 wafer format (166 × 166 mm^2) with multi-wire interconnection. The numbers of wires are varied from 18 (as standard for SHJ) to a reduced wire number of 9, 7, 5 and 3. Each wire has a physical diameter of

350 µm and an optical width of 210 µm due to back-reflection on the round wires.[21]

Starting with 18 wires, we compare the different finger metallization types. Figure 4 shows the cell efficiency within the module stack (i.e., P_{out} of Equation 1) for a silver screen printing paste as used for the SHJ baseline process (red, 220°C) which is, however, (currently) not applicable on a perovskite top cell. Additionally, we showcase P_{out} for a low-temperature paste with two different curing temperatures applicable to Perovskite cells of 150°C (yellow) and 130°C (blue); as well as for copper plating (green), where line resistivities are used as introduced in Section 2 (see Figure 1D or the legend in Figure 4). One can see that for 18 wires and an equal finger width of 35 µm, all finger metallization types (i.e., different line resistivities of the fingers) yield a similar efficiency. This is also reflected in the low series resistances R_S^{front} which is shown in Figure 4 on the right axis for the wires, fingers and TCO, respectively, in case of the Ag SP at 150°C. While the electrical losses due to wires and metal fingers are small, the 18 wires cause significant shading which is why we reduce the number of wires in a next step to find the optimum of the electro-optical trade-off.

For nine or less wires, both the series resistance of the finger R_S^{finger} (shown in grey for Ag SP at 150°C, right axis) and the wires R_S^{wires} (dark grey) are increased due to longer finger lengths towards the wires and less wires available for current transport, respectively. Still, we see that the overall module efficiency can be boosted since the optical gains are higher than the electrical losses. One can see that depending on the finger Ag SP process, either nine wires (for the low temperature paste at 130°C and 150°C) or seven wires (for Ag SP at 220°C) maximize the module efficiency (see stars labelled with their efficiencies), all for the 20-nm 'ITO3' and a finger pitch of 1.25 mm. Please note that the SHJ baseline process for Ag SP (at 220°C) is not applicable on perovskite up to this point due to its lower thermal stability. Copper plating (Figure 4, green) promises finger resistivities close to the intrinsic limit of bulk copper, which theoretically allows for even only five wires. However, please note that we have neglected the finger/wire contact resistivity which is typically small but could be critical when using a fewer wires. When using thinner wires with a diameter of 250 µm (not shown), the optimum number of wires to maximize the efficiency is shifted up towards nine wires (at slightly lower efficiencies), since the electrical losses within the round wires drastically increase while shading losses play a more subordinate role.

We conclude that the number of wires can be significantly reduced from 18 to 9 wires or even less depending on the finger metallization. Ag SP is feasible without major losses; however, a suitable ultra-low-temperature SP paste is necessary due to the lower thermal stability of the perovskite top cell. Plating could principally reach

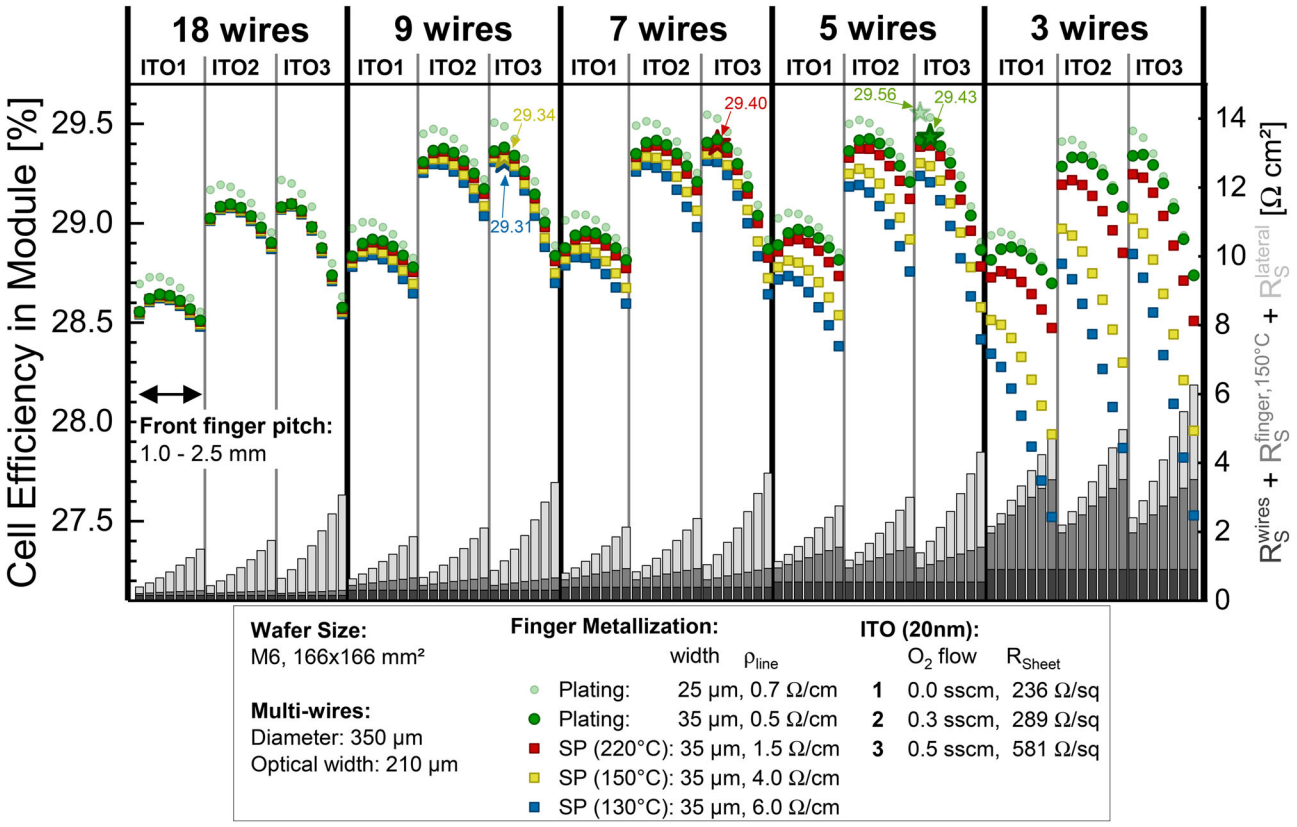


FIGURE 4 The cell efficiency in module (considering the monofacial module optics) for different numbers of multi-wires for the M6 cell interconnection and different finger metallization like plating and silver screen printing (SP) at different curing temperatures, as well as a variation of the front ITO properties (ITO1 to ITO3) and a front finger pitch variation between 1 and 2.5 mm (in each subsection). The right axis shows the contribution of the series resistances of wires, Ag SP finger (at 150°C) and the front TCO [Colour figure can be viewed at wileyonlinelibrary.com]

higher module efficiencies, especially when narrower finger widths are realized.

5 | COST ANALYSIS

Moving on with the optimized finger metallization and interconnection concept, we investigate the implications of the optimized front TCO and grid electrode on the module cost, silver consumption and levelized cost of electricity (LCOE). First, reducing the TCO thickness from standard 75 nm used in SHJ cells to the optimum of 20 nm is expected to reduce the cell production costs by 1.46 €ct/cell when using ITO as front TCO. If instead AZO is used as lower cost material for the front TCO, a thickness reduction from 75 to 20 nm would save around 0.79 €ct/cell.

Concerning the costs for the finger metallization, we focus on bifacial Pero-Si tandem cells, assuming 95 mg silver per rear side.[30,31] Figure 5 shows the module efficiency (yellow) for a monofacial module featuring 60 bifacial Pero-Si tandem cells with optimized TCO layer (20 nm, 'ITO2') on a nine multi-wire M6 wafer with Ag SP cured at 150°C as function of the front finger pitch. The module efficiency (in Figure 5) is about 2.6%$_{abs}$ lower than the cell efficiency within module (as shown in Figure 4) mainly due to considering the full module area with cell spacing and distance from frame to edge for a total module area of 1.8 m^2. One can see that the module efficiency reaches its maximum of 26.7% for a finger pitch of around 1.4 mm (marked as 'A' in Figure 5).

However, from an economical point of view, to save material resources and costs, we should also aim to reduce the amount of silver by increasing the finger pitch as shown in Figure 5, grey (right axis) by the front silver remaining (calculated based on the finger cross-section as in Figure 1D). Note that the silver consumption might be 5%–10% higher than the amount of silver remaining. On the other hand, this is counterbalanced by a reduction in module efficiency, which is why we should aim to also consider the levelized costs of electricity (LCOE). For the LCOE considerations, we use the same assumptions for the energy yield, production parameters, balance-of-system costs as in Messmer et al.[9] for the residential installation, although with updated process consumable costs which have changed in the meanwhile. For this work, we used a silver price of 25.87 $/oz and an n-type M6 wafer price of 65.3 $ct/wafer.

The LCOE (shown in Figure 5, blue, right axis) exhibits a minimum of 7.512 €ct/kWh for a front finger pitch of around 1.6 mm which is higher than the finger pitch for highest module efficiency (marked as 'B' in Figure 5). This LCOE is significantly lower than for a PERC single junction reference, where we obtain an LCOE of 8.49 €ct/kWh (not shown). The overall increased LCOE with respect to our last publication (where we yield LCOEs of around 6.6 €ct/kWh[9]) is due to the updated price scenario with currently higher wafer prices. Since this has influence on both single junction and silicon-based tandem devices, the Pero-Si tandem modules still yield a lower LCOE than silicon single junctions.

Figure 5 also shows the trade-off between module efficiency and silver costs: For a finger pitch of 1.4 mm (Figure 5, 'A'), we yield the highest module efficiency using 66 mg of silver on the front side. For 2.0 mm front finger pitch (Figure 5, 'C'), the module efficiency is slightly decreased by 0.08%$_{abs}$, but also the amount of silver on the front side is reduced by 20 to 46 mg. Both yield the same LCOE of

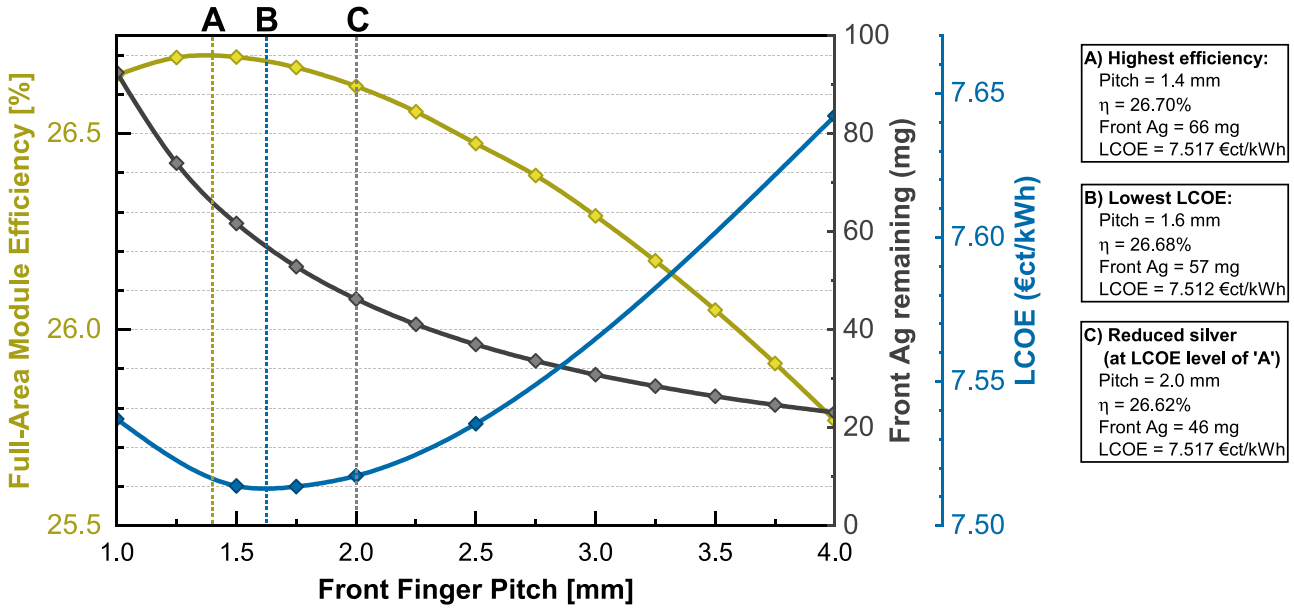


FIGURE 5 The full-area module efficiency (shown in yellow, including the back-sheet reflection of the monofacial module, cell and string interconnection losses and considering the full module area of 1.8 m^2) as a function of finger pitch, as well as the front silver consumption (grey), the front silver consumption per module output power (red) and the levelized costs of electricity (blue) [Colour figure can be viewed at wileyonlinelibrary.com]

7.517 €ct/kWh. We furthermore notice that the amount of silver on the front side with around 50 mg is comparable to the front silver consumption for SHJ single junction with multi-wire interconnection.[31] Therefore, we do not expect the front silver consumption for perovskite–silicon tandem devices to be significantly lower than for SHJ.

6 | CONCLUSION

We elaborated on how the front TCO and grid electrode for a perovskite–silicon tandem cell within a module must be adapted, using the learning of the recent years of SHJ single junction processing as a starting reference. Our optical simulations show that the different layer stack, in particular the refractive index of the perovskite absorber, facilitates the reduction of the TCO thickness down to its electrical limit (lateral transport and potentially contact formation with the paste) since it is no longer needed as ARC. This has the potential to reduce the parasitic absorption within the TCO while maintaining low reflection of the module.

At a first glance, lower resistive losses might be expected for a two-terminal tandem device since the TCO and grid electrode need to collect and transport only about half the current compared to a single junction device leading to only quarter the resistive power losses. However, we showcased that this higher series resistance tolerance is counterbalanced by three main factors: (i) an increased TCO sheet resistance which is due to its thickness reduction and possibly lower carrier mobility when non-ideal low-temperature deposition processes for ITO are applied, (ii) increased line resistivities for the low-temperature screen printed silver fingers, and (iii) higher share of the lateral current transport taking place within the TCO compared to an SHJ device due to the low lateral conductivity of the perovskite top cell.

Consequently, we conclude that the optimized front TCO electrode for a perovskite–silicon tandem cell should provide a thickness of around 10 to 20 nm (given that the contact formation with the silver paste is feasible). Also, the number of wires of the multi-wire cell interconnection can be reduced (similar holds for busbars) to nine or even less depending on the finger metallization and finger resistivity. For a finger metallization with very low-line resistivity, which can be potentially achieved with copper plating, a reduction down to five wires could be possible, given that the contact resistivity of the fingers towards the wires is low enough.

Subsequently, we elaborated on the implications of the costs and material consumption. For the TCO thickness reduction from 75 to 20 nm, we expect a cost reduction of 1.46 €ct/cell (0.79 €ct/cell) when using ITO (AZO) as TCO material. Furthermore, we showcased for an optimized monofacial module featuring 60 bifacial Pero-Si tandem cells that the optimum front finger pitch lies around 1.6 mm to minimize the levelized cost of electricity (LCOE) to 7.51 €ct/kWh which is still expected to be lower than for a respective PERC single junction (8.49 €ct/kWh). Increasing the front finger pitch to 2 mm has only minor impact on module efficiency and LCOE; however, the front silver usage can be reduced to about 50 mg/cell. This is comparable to the front silver usage of a SHJ single junction; thus, we do not expect a significantly lower front silver usage for perovskite–silicon tandem devices with respect to SHJ. Finally, we pointed out that the decrease in module efficiency with higher finger pitch is more pronounced in the Pero-Si tandem module than for a SHJ device, where the silicon bulk significantly contributes to the lateral transport. The latter motivates the need for thin TCOs with excellent mobility to keep the TCO sheet resistance and hence Ag consumption on a moderate level.

ACKNOWLEDGEMENTS

This work was supported as a Fraunhofer Lighthouse Project (MaNiTU). Furthermore, Christoph Messmer would like to thank the 'Deutsche Bundesstiftung Umwelt (DBU)' for funding his dissertation project. The authors are responsible for the content.

DATA AVAILABILITY STATEMENT

Research data are not shared.

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How to cite this article: Messmer C, Tutsch L, Pingel S, et al. Optimized front TCO and metal grid electrode for module-integrated perovskite–silicon tandem solar cells. *Prog Photovolt Res Appl*. 2021;1-10. doi:10.1002/pip.3491