SINGLE SIDE POLISH ETCHING FOR THE REAR SIDE OF CRYSTALLINE SILICON WAFERS

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ABSTRACT: Standard silicon solar cells have a textured front and rear side. In order to optimize the light trapping within the cell and the conditions for a good rear side passivation with local contacts, a planar rear surface is most suitable. The different structured front and rear surfaces of the wafer make the implementation of a single side etching process step essential. The main focus in this study is etching a planar rear surface with industrial standard applications based on a textured surface. With isotropic etch behaviour and high etch rates, which are preferred for inline processes, acidic measures are used to flatten the rear surface of the wafer. Mono- and multicrystalline wafers have been etched by obtaining a weighted reflection of about 35%. A successful single side polish etching after texturization requires a high silicon removal (10 to 30 µm). This process was already successfully transferred to an industrially deployable highly efficient cell design.

1 INTRODUCTION

Currently in the photovoltaic industry there is a trend toward cost-driven wafer thinning for crystalline silicon solar cells. Wafer thinning leads to an increase of the ratio of the wafer surface to volume and therefore, a good front and rear surface passivation is essential for obtaining low surface recombination velocities. Moreover, a good surface passivation will lead to higher solar cell efficiencies. This is caused by increasing the internal reflection (light trapping), decreasing recombination on the rear side and less chemical stress between silicon and metallization. A high reflection of transmitting radiation on the rear side of the cell is another benefit to a flat surface structure which becomes more important for thin wafers. Many high efficiency cell designs imply a passivated and locally contacted rear surface (PERC), which requires an etched emitter and a flat surface on the rear side. Currently standard industrial cell designs obtain a textured surface on both sides [1].

The challenge of this study is to develop a successful industrially suitable single side polish etching process with a subsequent characterization of the polished surfaces. For the development of the process, an industrially suitable inline etching system could be used at the Photovoltaic Technology Evaluation Center (PV-TEC) at Fraunhofer ISE.

2 EXPERIMENTAL DETAILS

2.1 Sample preparation and pretests

The experiments were performed using p-type mono- and multicrystalline silicon wafers with an area of 156 x 156 mm^2, and a thickness of 140 to 300 µm. The main focus was on Cz <100> oriented silicon wafers with random pyramids and a weighted reflection of approximately 12%. The multicrystalline material had been textured by an acidic isotexture with a weighted reflection of 24% to 30%.

The etching solution was adjusted in beaker experiments with highly concentrated acidic solutions in order to reach a high silicon removal. Mixtures of HF, HNO_3 and CH_3COOH have been investigated. These investigations have been performed in beaker batch experiments with a cooled mixture. The 2 x 2 mm^2 surfaces have been characterized by etching rate, weighted reflection and confocal microscopy.

2.2 Single side polish process

All wet chemical single side etching experiments have been performed on a modified industrial inline texturization system by Gebr. Schmid GmbH, Freudenstadt, Germany. The system contains the etching module for hydrofluoric acid (HF), nitric acid (HNO_3), acetic acid (CH_3COOH) and several cleaning steps that can be optionally switched on. After the polish process the wafers where cleaned by using all cleaning sequences.

The single side process uses transportation rolls on which the wafers lay. There is no upper transport system and the wafers remain on the transportation rolls only by gravity. The solution level below the wafers can be adjusted. The textured wafers have a hydrophobic surface and therefore it is possible to etch them in a “swimming” process without requiring a wrap around. This is realized due to the meniscus between the acidic solution and the wafer surface on the lower side. This meniscus is only possible at transportation velocities < 1.5 m/min. At transportation velocities between 1.5 to 1.7 m/min, the meniscus will break away. At velocities < 0.5 m/min, especially in the case of thin wafers < 150 µm, wafers can stick or turn in the polishing module caused by the reaction gas bubbles which occur at the etched lower side of the wafer.

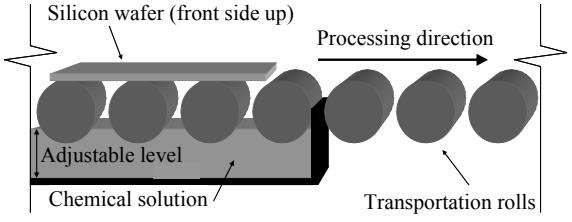

Figure 1: Schematic illustration of the used industrial single side process. The solution level is adjustable up to the lower side of the wafer.

To avoid a modification to the emitter on the front the polishing process must take place before the diffusion

process. After the diffusion the silicon surface is hydrophilic, what leads to wrap around and an attack of the front emitter. This is due to the acidic and chemical reaction gas phase for high silicon removals.

2.3 Surface characterization

The surfaces of the single side etched wafers were characterized by confocal microscopy, weighted reflection and SEM micrographs. The weighted reflection of the polished silicon surface is only significant at texture angels above 30°. Below 30° the reflection is equivalent to that of a polished wafer (≈ 35%). To characterize the surface structure using weighted reflection is only possible to an angle above 30° [3]. For further surface characterization the following statistical roughness parameters were used [4]. These parameters are based on spatially resolved height data from a confocal microscope.

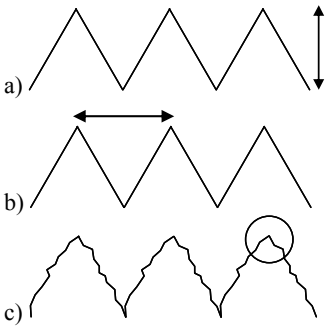

Figure 2: a) Root Mean Square Roughness (RMS). Measure of the vertical peak height values.
b) Lateral Correlation Length (ξ). Measure of the horizontal distance between the peaks.
c) Roughness exponent (α). Measure of the mirco roughness. α between 0 and 1. In the case of roughness exponent equal to one there is no micro roughness [4].

3 RESULTS

3.1 Pretest

Several experiments have been performed to flatten the texture and polish the rough surface. In small acidic batch experiments we could identify that a fast and high rate of silicon removal was the significant effect of a flat surface. Therefore a high flux on the surface is needed to afford a replacement of the etching solution at the wafer surface.

To transfer a small scale experiment to an industrial application, the same proportion between etched silicon surfaces to the volume of etching solution is necessary. Otherwise, the solved reaction products that rush the reaction are less concentrated because of the lower etched silicon surface ratio to volume in an industrial plant.

3.2 The acidic etching system

The isotropic acidic etching solution is a mixture of HF, HNO_3, CH_3COOH and ultrapure water. The CH_3COOH lowers the dielectric constant of the water, which results in less dissociation of HNO_3 and hence a greater degree of oxidation. In addition, it helps to have a proper wetting of the hydrophobic textured silicon wafer surface.

During the acidic reaction of HF/HNO_3 with the SiO_2 surface, hexafluorosilicic acid (H_2SiF_6) will be produced, which increases the etch rate and is more useful to polish the surface. Furthermore, the etch rate rises up to a plateau with the amount of solved nitric species (NO_2, N_2O_3, $[N_4O_6^{2+}]$) that are products of the chemical reaction. This is indicated by the yellow colour of an old etching solution. Therefore we enhance the etching solution by dissolving dummy wafers prior to the polishing process. The solved nitric species will exponentially decrease over time at atmosphere [2]. Therefore it is necessary to repeat the solving preparation by using dummy wafer after a long term without processing.

The etch process is very fast (etching rate ≈ 2 to 20 µm/min) and therefore practical for industrial applications. The etch rate can be adjusted by the concentration of the mixture, as well as by the temperature or wafer velocity. The etch rate is also controlled by the solved nitric species and the hexafluorosilicic acid. These two reaction products, especially the solved nitric species, can be enriched by using dummy wafers in advance. The wafer velocity has to be adjusted to reach a desired silicon removal without causing the wafers to turn by the reaction gas bubbles, which occur under the wafers and escape them on the rear edge.

3.3 Surface characterization

As the etch amount is important, the etch depth during the polishing process was varied. The wafers pass the polishing process with individual velocities to evaluate the possibility of maximum reflection with the available application (Fig. 3).

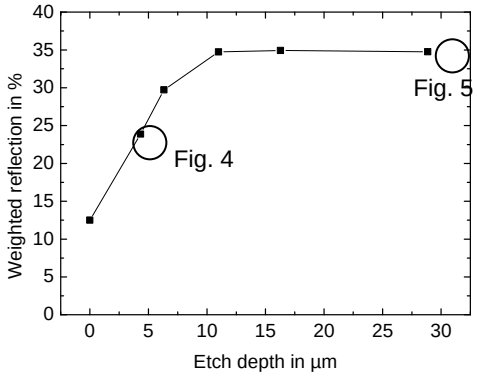

Figure 3: Weighted reflection after the polishing process versus silicon removal during polishing process. Cz-Si feed material with random pyramids. Above 12 µm etch depth the reflection is constant.
The weighted reflection reaches a plateau at about 35%. This is due to the surface structure angle below 30° at a etch depth above 12 µm.

The textured and polished surfaces were analyzed by measuring the height profile of the wafer surface with a confocal microscope (Fig. 4 and 5).The surface with a 4.3 µm etch depth has a 10 µm span, with a etch depth of 28 µm the span is reduced to about 4 µm.

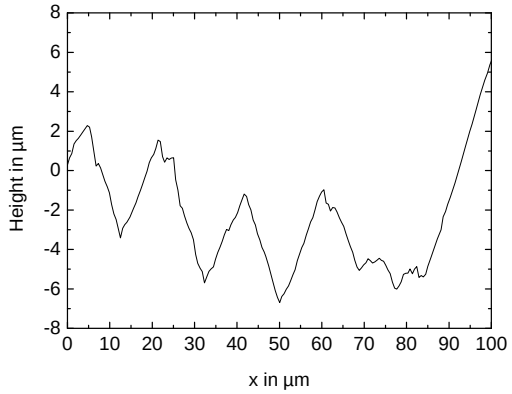

Figure 4: Height profile of a Cz-Si wafer with an etch depth of 4.3 µm. Same wafer as in Fig. 3.

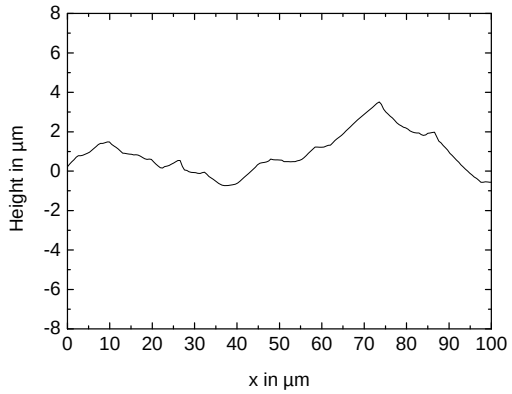

Figure 5: Height profile of a polished Cz-Si wafer with an etch depth of 28.9 µm. Same wafer as in Fig. 3.

The surface flattening is still in progress after the plateau of maximum weighted reflection at about 35%. To characterize the wafer surface at 35% weighted reflection the three statistical roughness parameters of Fig. 2 are used.

The RMS roughness refers to the vertical peak height of the surface structure (Fig. 6, top). The RMS drops from 2.3 ± 0.1 µm to 1.3 ± 0.2 µm at the same level of weighted reflection.

A reduction of the peak height in combination with a larger distance between the peaks, which is expressed by the lateral correlation length, is the main characteristic for the modification from a textured to a polished surface (Fig. 6, center).

The roughness exponent (α) is the measure for the micro roughness of the surface (Fig. 6, bottom). The exponent is between 0 and 1. There is no micro roughness in the case of roughness exponent equal to 1. A lower micro roughness is most suitable for a good passivated surface.

The etching depth limit with the available inline application is at about 30 µm. This is due to the single side module length of the used plant. The surface structure is isotropically enlarged by further etching depths. For Cz material, an economic optimum at 15 µm etch depth is found.

There is a difference for the polishing process between anisotropic etched random pyramids of Cz-Si and isotropic etched multicrystalline surfaces which should be flattened. To reach a high reflection, which correlates to a roughness with low vertical peak height, a silicon removal at least greater than the texture height is required. The required etch depth is dependent on the texturization morphology, i.e. the pretreatment of the Si-feed wafers. Therefore it is obvious that the etch depth has to be greater at a surface with big pyramids instead of small pyramids or an acidic textured surface.

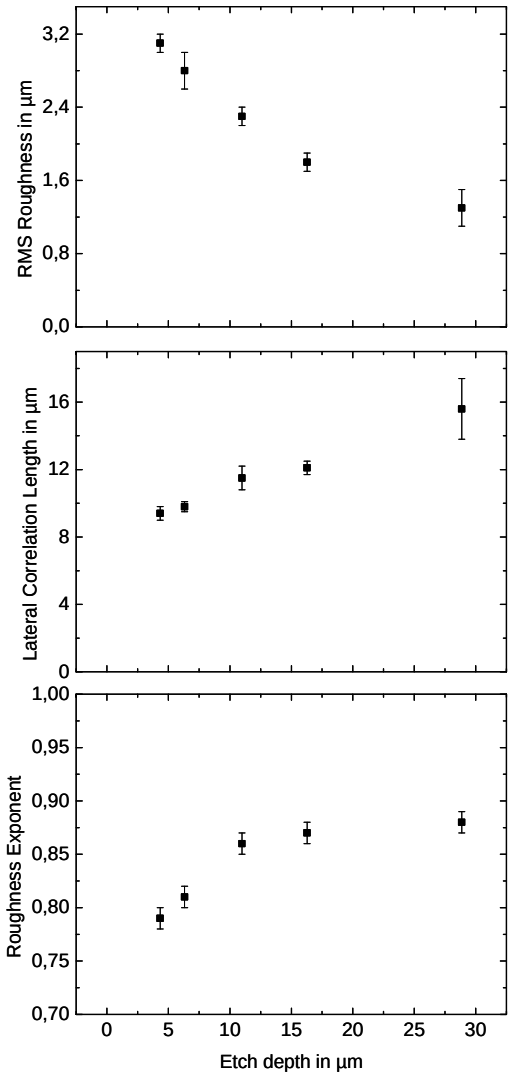

Figure 6: Statistical surface characterization measurements of the polished Cz-Si Wafers at different etch depths (n=3 measurement points on one wafer). Root Mean Square (RMS) roughness (top). Lateral correlation length (center). Roughness Exponent (α) (bottom).

3.4 Comparison of polished mono- and multicrystalline silicon

The investigations above have all been realized with 156 x 156 mm^2 Cz-Si. The samples are all textured with random pyramids. The effect on multicrystalline material was also checked. The isotexture on the used multicrystalline wafers of different suppliers have a weighted reflection from 24 to 31%. A smaller benefit in reflection increase can be expected in comparison to Cz-Si feed material. The typical acidic textured surface changed from small topography to large sockets (Fig. 7).

In the resulting surfaces at a etch depth of about 15 µm for mono- and about 10 µm for mulicrystalline feed material the surfaces are similar (Fig. 7). The random pyramids of Cz-Si material are changing within the etch depth from a structure with defined sharp edges to a surface with rounded structures. To remove all pyramids completely a etch depth of about 15 µm is required for Cz-Si.

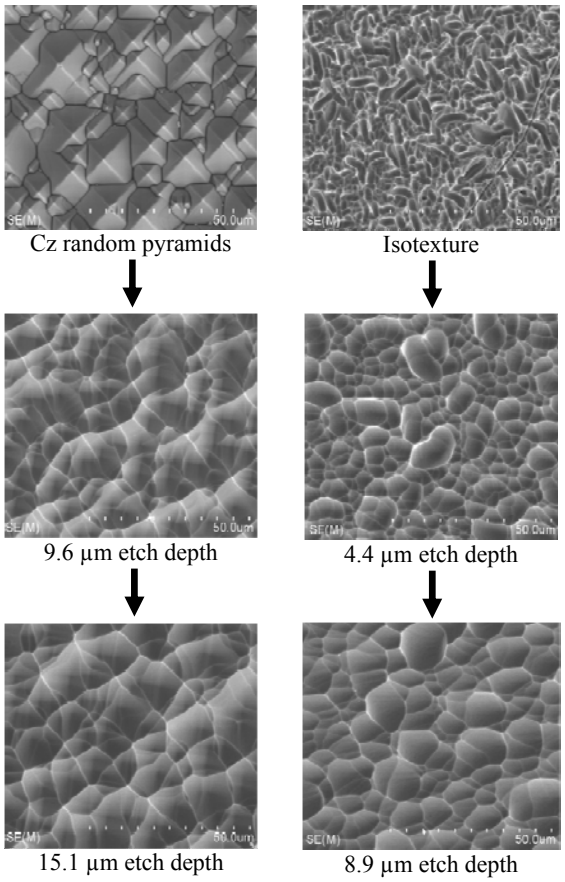

Figure 7: SEM images of textured and polished Cz wafers (left) and multicrystalline wafers (right) at different etch depths. With increasing the etch depth the surface structure of monocrystalline material ends in a similar morphology as multicrystalline material.

With increasing the etch depth on multicrystalline isotropically textured surfaces, the resulting morphology ends in a similar structure as monocrystalline material. As expected on multicrystalline material, a lower silicon removal is required due to the smaller isotropic texture height. The economic optimum for multicrystalline textured material is a 10µm etch depth.

4 SUMMARY

In this study an acidic polishing process with HF, HNO_3 and CH_3COOH at an industrial scale inline etching plant was presented. Polished mono- and multicrystalline wafers at different etch depths were characterized. With increasing the etch depth the flatness of the structure increases. This could be seen in the decreasing Root Mean Square and increasing lateral correlation length. This could additionally be certified by SEM images. The best results regarding the needs of economics and industrial reliability was at 10 µm for multi- and 15 µm for monocrystalline material. With this process, industrial cell designs up to 19% efficiency have already been realized [5].

The combination of the single side polishing together with parasitic emitter removal is beneficial for the decrease in solar cell manufacturing steps, and therefore in lower processing costs as well. This is the challenge for further development.

5 ACKNOWLEDGEMENTS

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