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Benefits of different process routes for industrial direct front side plating

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Abstract

In this work, we highlight the benefits of alternative plating routes compared to the standard plating route primarily discussed in literature and currently introduced in pilot production [1, 2]. The common plating route starts with the laser ablation of the front side grid after rear side Al-printing and firing. Then, an HF dip removes the native oxide for the subsequent light induced Nickel-, Copper plating (LIP) with a Silver capping as a finishing. Afterwards, an annealing step improves the adhesion of the plated grid and its contact resistance. Here, we want to show the advantage of three alternative process routes. In the first alternative route, the laser opening of the front side grid is performed before the firing step. During firing, the laser damage is partly cured and can lead to an increase in open circuit voltage (V_{oc}) of 7 mV on state of the art industrial PERC solar cells. For the second process route, the removal of the native oxide is eliminated. To achieve this, special laser and plating conditions are needed. Finally, for the third alternative process route, the annealing of the plated stack can be combined with a stabilization process supressing the light induced degradation (LID). The presented alternative routes give new degrees of freedom for process optimizations regarding precursor-induced features such as high laser damage on shallow emitters, parasitic plating (PP) for passivation layers with high pinhole density or LID.

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Keywords: metallization; copper plating, structuring, contact formation

1. Motivation

PERC solar cells are becoming mainstream in solar industry. Consequently, the front side becomes the main efficiency-limiting factor. The copper plating technology has the potential to reduce cost and improve efficiency, and hence become the next generation metallization. In combination with laser opening it allows finger widths as narrow

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as 15 µm on an industrial scale. With the standard route, we achieved 21.2% cell efficiency on industrial Cz-Si PERC cells with homogeneous emitter and a cell area of 240 cm². However, this cell efficiency is still limited by a higher damage of the front contact compared to screen printing and PP.

1.1. Different plating routes

For plating the standard process route of Al-BSF and PERC solar cells starts after the printing and firing step of the backside. In Figure 1 the different process routes are shown.

Route	Process Steps					Advantages
Standard	Al print and FFO	LCO Front Grid	HF Dip	Ni/Cu/Ag plating	Anneal	well known
A) Laser damage curing	LCO Front Grid	Al print and FFO	HF Dip	Ni/Cu/Ag plating	Anneal	higher Voc
B) Easy Plating	Al print and FFO	LCO Front Grid	-->	Ni/Cu/Ag plating	Anneal	PP protection
C) integrated LID curing	Al print and FFO	LCO Front Grid	HF Dip	Ni/Cu/Ag plating	Anneal + LID recovery	LID stabilized

Fig. 1. Four possible process routes for the plating cluster

For the standard approach the first new process step after printing and firing of the rear side is the laser opening of the front grid followed by a HF dip to remove the native oxide and subsequently Nickel, Copper, Silver plating. Finally, the plated metal stack is annealed to form a low contact resistance and an adhesive metal stack [1, 2]. In this publication, we will discuss the advantage of alternative process routes. For example A) the firing step can be used to cure laser induced damage. B) For the easy plating route, the HF dip is omitted to avoid unwanted parasitic plating. C) Ultimately, the annealing furnace can be combined with a LID recovery system.

2. Experimental

2.1. Alternative route A) Laser damage curing

It has been shown that the laser damage can be partly cured during the firing step [3]. Here, we demonstrate the potential of the laser damage curing on state of the art industrial PERC precursors. The same upstream process up to the rear side aluminium screen printing, was applied to all wafers. Then the cells were split into two groups. One was manufactured with the standard route and the other according to route A). In FIG. 2a) the V_{oc} and b) the efficiency of the finished cells are shown. The group, which underwent the laser damage curing route, shows an average V_{oc} and efficiency increase (compared to the reference group with the standard process route) of 7 mV and 0.2 %, respectively.

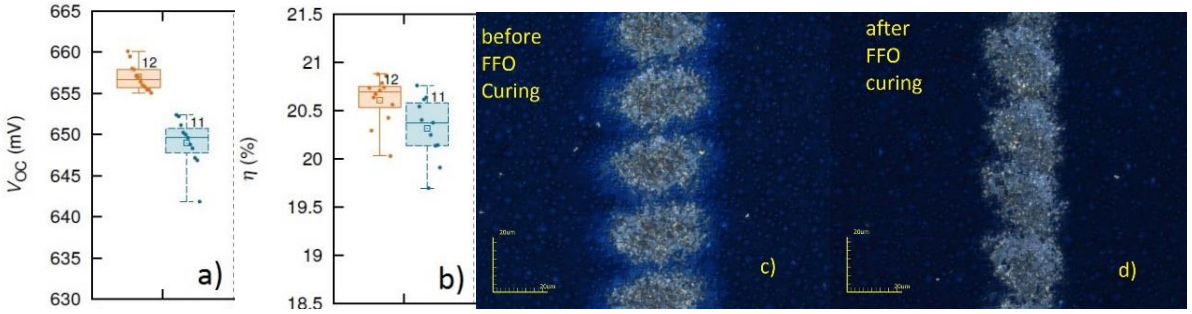

Fig. 2. a) V_{oc} and b) efficiency of PERC solar cells. In blue is the Standard process route and in orange the alternative route A) is shown. Microscope picture direct c) after laser front opening and d) after FFO anneal

FIG. 2 c),d) shows microscope images of a UV picosecond laser opening. Image c) was taken directly after the laser patterning and image d) was taken after laser patterning and a standard fast firing process (FFO). The light blue area around the opening consists of amorphous silicon underneath the remaining anti-reflection layer, which is created by rapid cooling due to the peripheral illumination using a Gaussian laser spot profile. When applying a standard FFO process, the majority of the amorphous silicon is recrystallized and the area is observed as dark blue again, which results in lower recombination in the contact area [4]. Another possibility to reduce the laser-induced damage is an in-situ nanosecond laser annealing, [5] or the use of a selective emitter with a good minority carrier shielding.

2.2. Alternative route B) Easy Plating

In the so called "Easy Plating" process route, the removal of the native oxide before the Ni/Cu/Ag plating is omitted. This has the advantage that pinholes are not activated, and will not be plated. A detailed process explanation can be found in [6,7,8]. This approach prevents parasitic plating on area with unintentionally damaged SiN_x and allows the usage of standard SiN_x depositions without any special protection against parasitic plating [9]. In Figure 3 the easy plating process is visually compared to the standard plating route. The top pictures show a high resolution scan. With the standard plating route, parasitic plating is visible, but not with the easy plating route. The pictures at the bottom show automatically detected parasitic plating structures. The red area indicates parasitic plating. This method allows a quantitative analysis of parasitic plating and an efficiency loss caused by parasitic plating can be calculated [7]

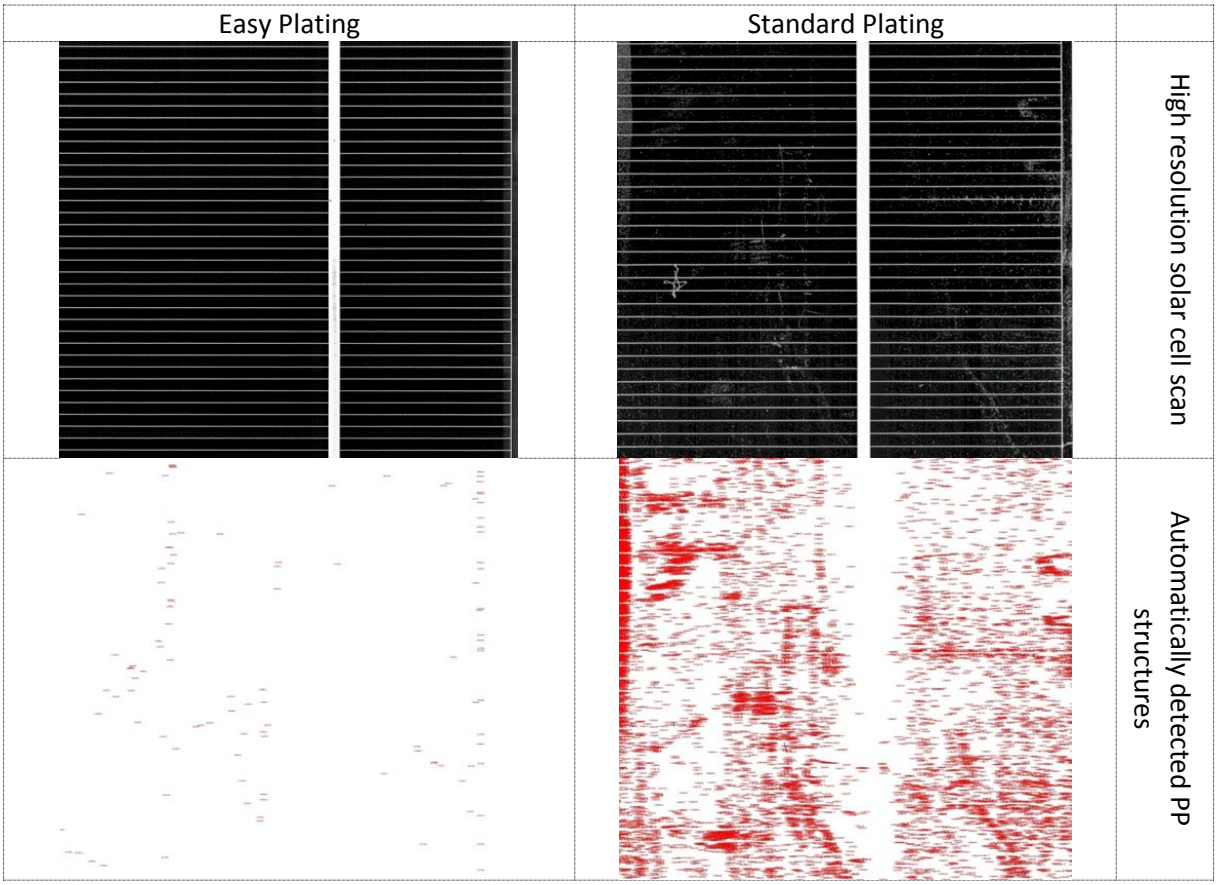

Fig. 3. Top) High resolution solar cell scan pictures and Down) automatically detected PP structures of left) easy plate and right) standard plating.

We have tested the easy plating route on four different cell precursor types. The cell precursors were produced at different industrial production lines and they used the same front end process as their screen printed production cells. Material 1,2,3 are cz-Al-BSF cells. Material 4 are mc-PERC cells. On precursor 1,4 a high amount, on precursor 2 a medium amount and on precursor 3 a very low amount of parasitic plating was observed for the standard plating route. In Fig 4 the standard route is compared with the easy plating route B) in the electrical parameters J_{sc}, R_s, Efficiency and Busbar Peel-Off Force after soldering. As expected, the highest J_{sc} gain can be achieved with a material with a high parasitic plating amount (precursor 1 and 4). On precursor 3 with a very low parasitic plating the easy plating route shows no gain in J_{sc}. We can conclude that for a well optimized production line and when all wafer handling steps are fully automated (precursor 3), the easy plating approach is not necessary and beneficial. In this experiment, the easy plating route B) shows only on Material 1 a good contact resistance.

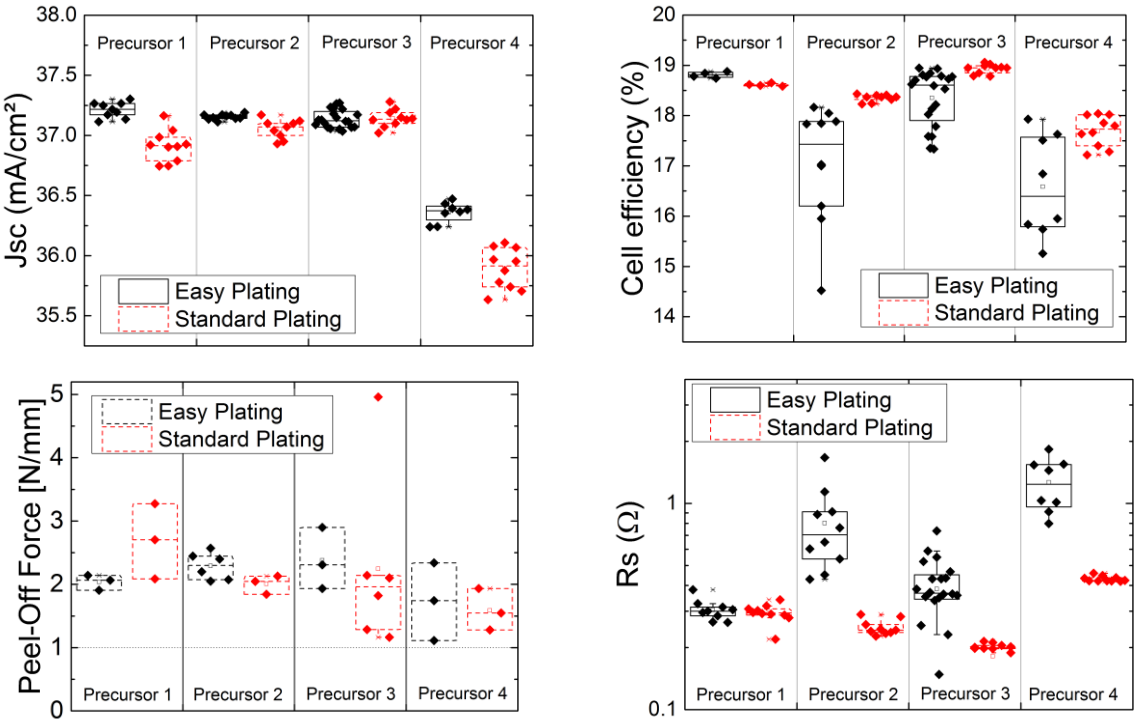

Fig. 4. The easy plate route B) is compared with the standard plating route on four different precursor types in the cell parameters J_{sc}, Efficiency, R_s and the Busbar Peel-Off Force.

Careful selected laser and plating parameter adapted for the easy plate process route allow an adhesive nickel deposition with a good contact resistance. It is shown that it is possible to achieve a higher efficiency and metal adhesion with route B on Material 1. We want to emphasize that Material 3 is manufactured in a state of the art production line without any special optimization for plating and that the appearance of all cells with the easy plating route is very good. Further work needs to be done to fully understand how to create a good contact resistance on a variety of precursors.

2.3. Alternative route C) Combination of anneal and LID stabilization

The annealing step after plating improves the adhesion of the plated contacts to the silicon, decreases the contact resistance at the Si/Ni interface, and lowers the bulk resistivity of the plated copper. Usually, the annealing is

performed in an inline furnace with nitrogen atmosphere and heated by heating coils. With a simple substitution of the heating coils by infrared lamps, a LID stabilization can be obtained. For the conducted experiment, we use standard industrial p-Type Cz-Al-BSF precursors. After opening the front side with an UV-ps laser and light induced plating, the cells were annealed by IR-lamps heating to 225/ 250 and 275 °C for 1/ 2/ 5 and 10 minutes. A reference group was annealed with heating coils. Afterwards all cells were degraded at room temperature under 0,5 suns for 3 days. Table II shows the V_{oc} and J_{sc} values of cells of route C and the standard route as a reference. It is shown that, with a simple substitution of the heating coils by Infrared lamps, a stabilization of about 70% against LID can be reached. We estimate a higher stabilization on PERC solar cells with this process.

Table 1. J_{sc} and V_{oc} values of route C) and the standard route as a reference measured after annealing and after LID.

	Route C) annealed with infrared lamps and different parameters (23 cells)		**Standard route** with heating coils as a reference (7 cells)	
Measurements taken:	V_{oc} (mV)	J_{sc} (mA/cm²)	V_{oc} (mV)	J_{sc} (mA/cm²)
After annealing	638 ± 1	37 ± 0,1	638 ± 2	37,1 ± 0,2
After Light induced degradation	633 ± 2	36 ± 0,2	624 ± 3	36,1 ± 0,2
Absolute Loss caused by LID	**5 ± 1**	**0,3 ± 0,1**	**14 ± 2**	**1 ± 0,2**

4. Conclusion and outlook

We have developed three alternative plating routes, which have the potential to increase the efficiency and/or simplify the process, and hence save production costs. Already with the standard route, a cell efficiency of 21.2 % on industrial PERC cells was achieved. With the laser damage curing A) an increase in V_{oc} of 7 mV and an efficiency of 0,2% was achieved. The easy plating route B) allows plating without parasitic deposition even if passivation layers with a high pinhole density are used. As shown in route C) LID stabilization can be realized in the annealing step by introducing infrared light in the furnace. Process route C) can be combined with A) and B). A combination of A) and B) is not possible, but by using a selective emitter with a good shielding, the advantage of route A) becomes negligible. This allows fabrication of a plated cell with low $J_{o,contact}$, no PP, and stabilization against LID.

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