Design support for 3D-Integration by physical oriented modeling of interconnect structures

Peter Schneider[1], Sven Reitz[1], Andreas Wilde[1], Jörn Stolle[1]
Josef Weber[2], Peter Ramm[2]

[1]Fraunhofer Institute for Integrated Circuits,
Design Automation Division

[2]Fraunhofer Institute for Reliability and Microintegration,
Munich Division

Email: peter.schneider@eas.iis.fraunhofer.de

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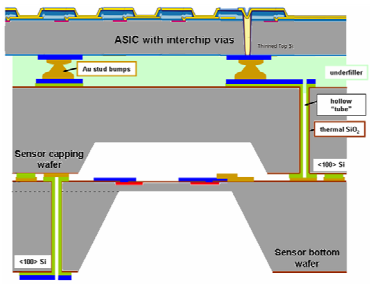
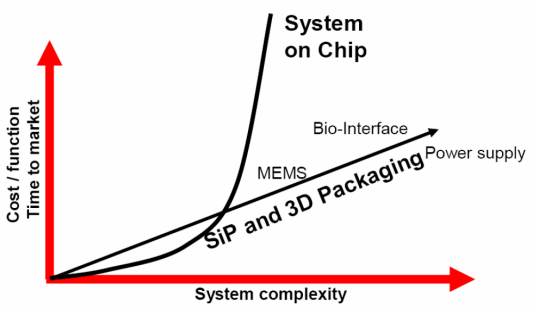
Outline

- **Introduction**
- Methodology for multi-level and multi-physics analysis of interconnect structures
- 3D Integration process based on ICV-SLID
- Thermal analysis and electro-thermal simulation
- Modeling of electrical behavior at low and high frequencies
- Design flow integration and system level simulation
- Conclusions

Key elements of SiP / 3D integration technology



Source: SINTEF



Source: ITRS-Roadmap 2005

- system partitioning/modularization
- chip-package co-design (on chip, off chip)
- integration of different functions in one package
- application of "add-on" technologies
- high-density component integration
- short time to market cycles

3D Integration – Impact on System Behavior

Very high density of inter-chip wiring and functional blocks

leads to some physical effects with influence on device functions and system behavior:

– signal integrity

– cross talk

– interconnect delays

– power and thermal behavior

– thermo-mechanical issues

Design of 3D systems is a multi-criteria optimization problem !!!

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Methodology for multi-level and multi-physics analysis of interconnect structures

Goal

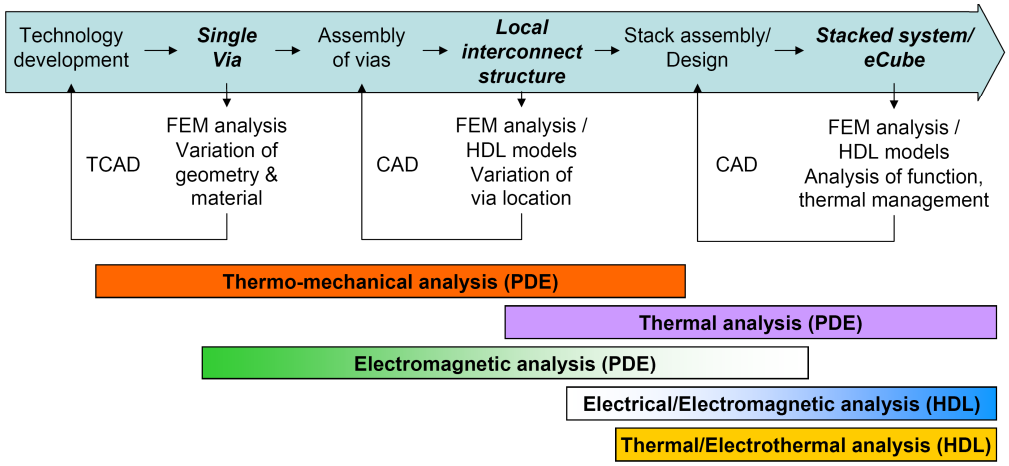
Derive information from integration technology and provide it for system design

Basic elements

1. Modular modeling approach
2. Simulation on component level, e.g. using FEM
3. Methods for computer-aided model generation for system level (reduced order modeling)
4. Model validation
5. Integration of equivalent circuit or behavioral models into the design flow
6. Derivation of design guidelines for interconnect structures

Methodology for multi-level and multi-physics analysis of interconnect structures

Modular Approach for Modeling and Simulation



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Representation of structures

Tool independent descriptions of basic structures

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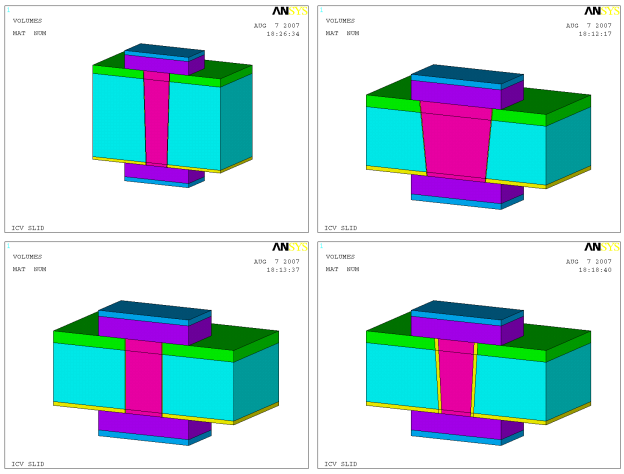
Geometry
Material
„Physics“
Mesh quality

Model generation

FEM models for ICV-SLID with different geometry



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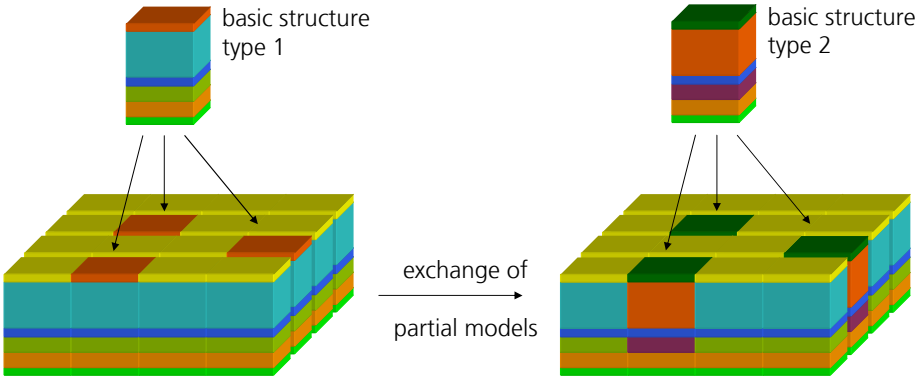
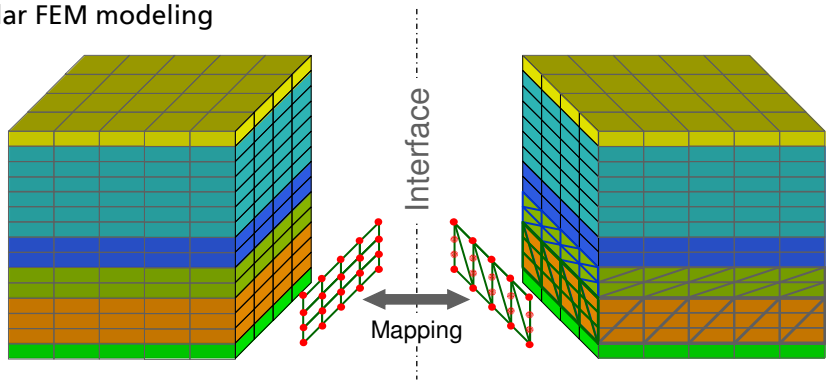
Representation of structures

Modular FEM modeling



Representation of structures

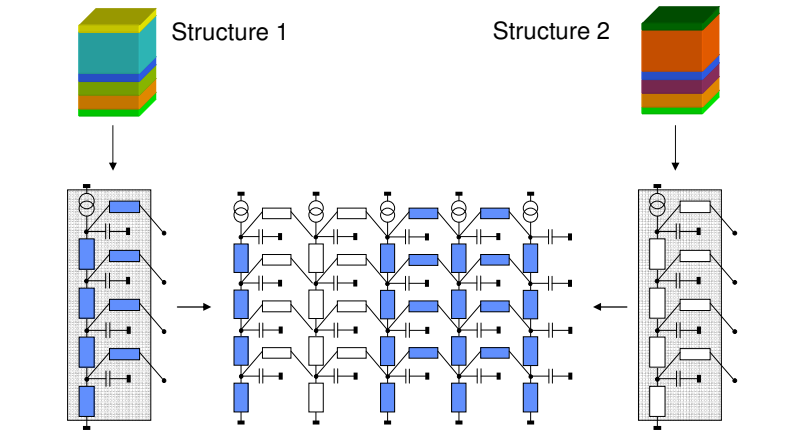
Modular FEM modeling



- Layer thickness
- Material properties
- Finite element mesh
- Element types / DOFs
- Boundary conditions

Representation of structures

Modular system level modeling – equivalent circuit and/or behavioral model



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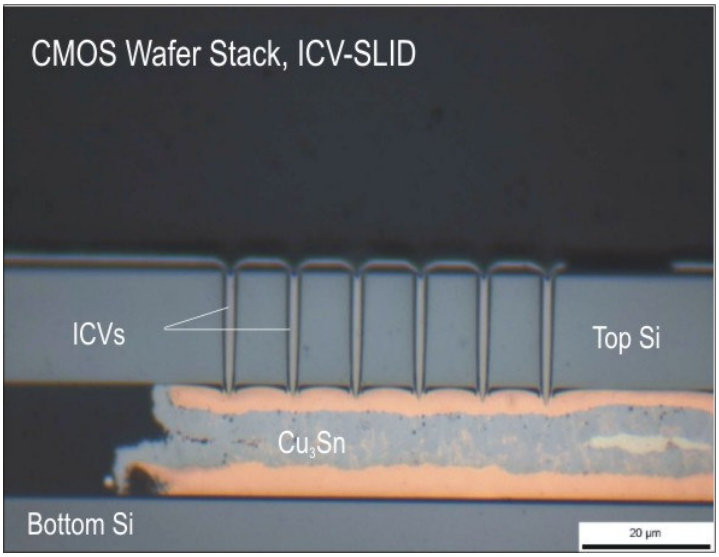
ICV-SLID Technology (InterChip Via – Solid Liquid InterDiffusion)



3D integrated CMOS device stack (micrograph) showing tungsten – filled through-silicon-vias (ICVs) and Cu-Sn-Cu Metal system building the stable intermetallic Cu_3Sn phase by Solid-Liquid-InterDiffusion (SLID)

(Source: Fraunhofer IZM Munich)

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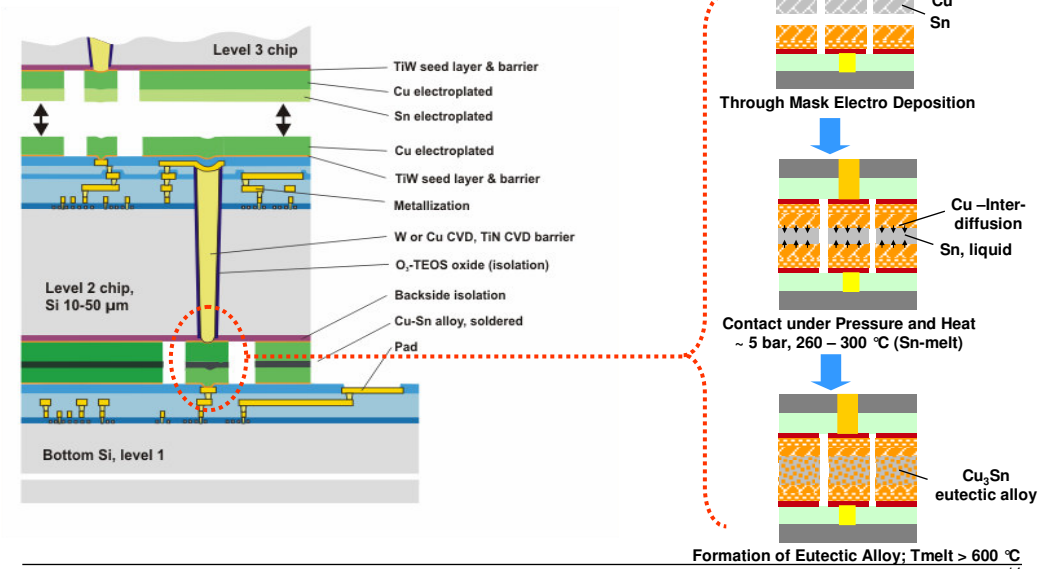
SLID: Solid-Liquid Inter-Diffusion

Simultaneous formation of **electrical and mechanical** connections



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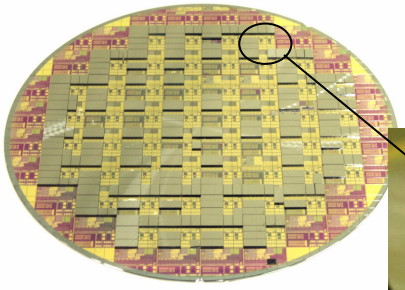
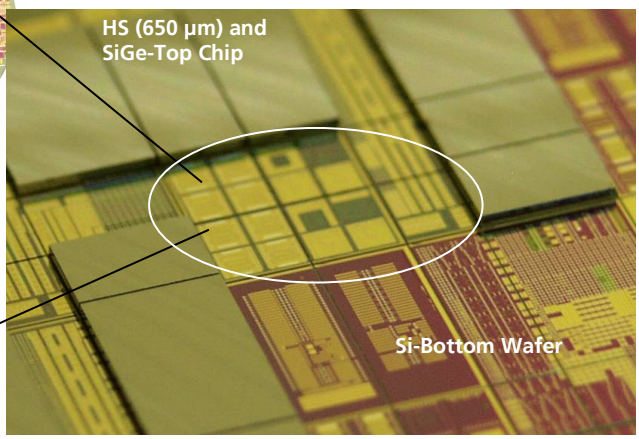
Chip-to-Wafer Stacking by ICV-SLID Technology



Vertical System Integration of CMOS-devices in strained Si/SiGe-Technology (Topchip) and Si-technology (Bottom-Wafer)



Top SiGe chip, 20 µm thick, stacked on bottom Si device, handling substrate (HS) removed

(Source: Fraunhofer IZM Munich)

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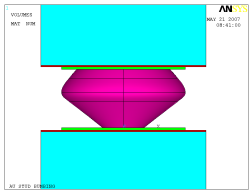
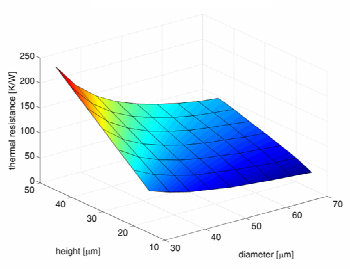
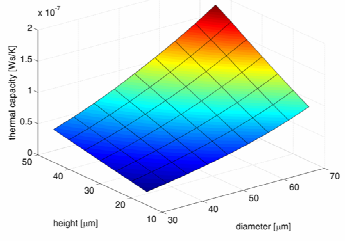
Thermal simulation

Thermal characterization of different interconnect technologies

Au stud bumps

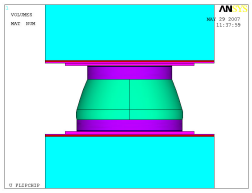


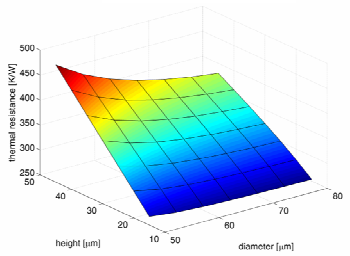


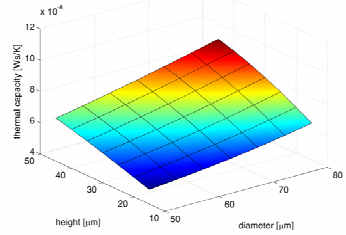


Thermal resistance **Thermal capacity**

µ-flip-chip







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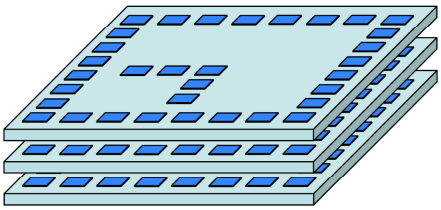
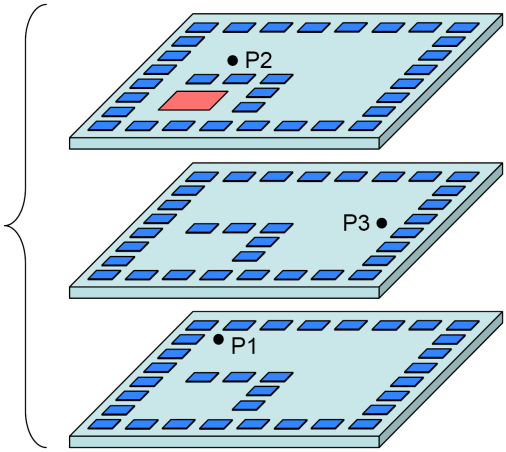
Thermal simulation

Thermal analysis of entire stack structure

Stack structure with vias for heat spreading



Stack layers with heat source (red square) and sensitive devices at P1, P2 and P3



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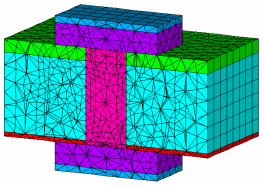
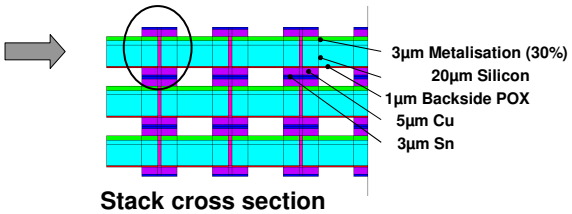
Thermal simulation

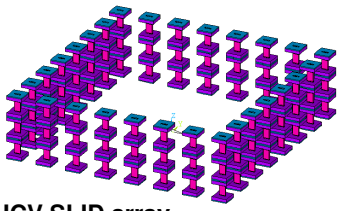
Modular modeling of stack structure



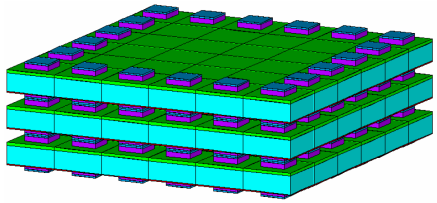
ICV SLID



Stack cross section



ICV SLID array



Stack model

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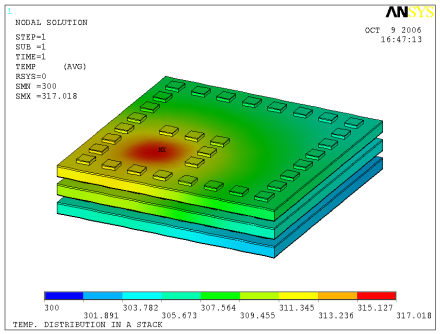
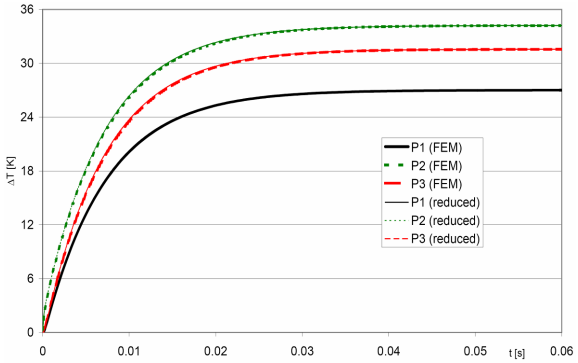
Thermal simulation

Results of FEM and system level simulation

FEM simulation with ANSYS



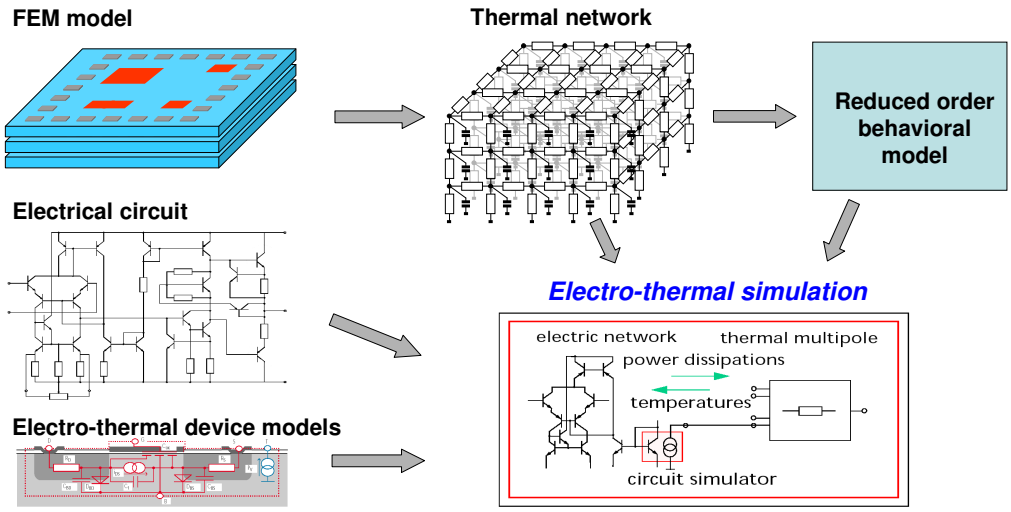
System simulation with reduced order model



System level model for thermal system:

- 40 system variables
- derived from FEM description with 95,000 system variables by model order reduction
- Simulation carried out with SABER

Electro-thermal simulation



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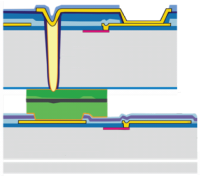
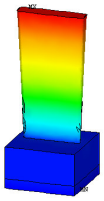
System level modeling

ICV structure

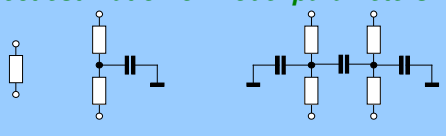


FEM results

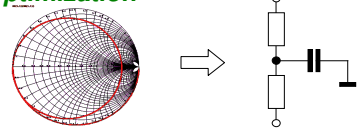


FEM model
(equations)

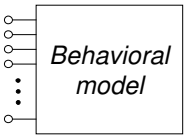
Direct estimation of model parameters



Optimization

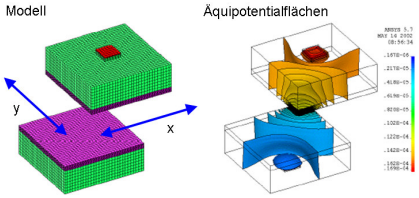


Order reduction



VHDL-AMS,
Verilog-AMS,
SystemC-AMS,
…

Calculation of circuit parameters



Field calculation

network model

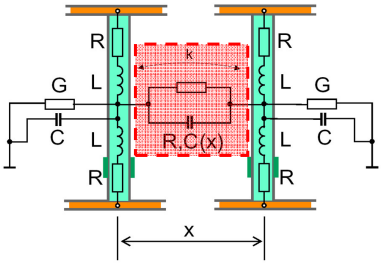
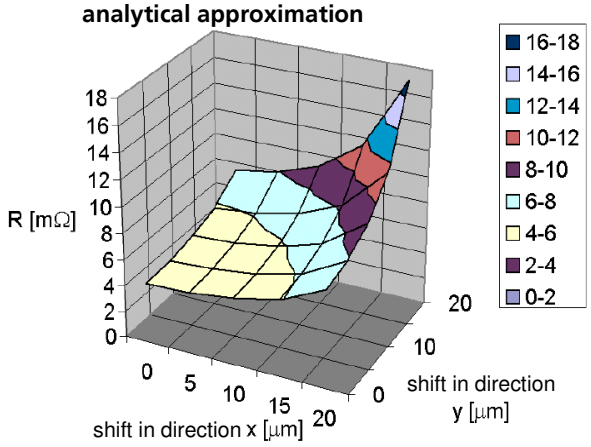


Table models or analytical approximation



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Electrical behavior at high frequencies

Necessary

- Frequency dependent values of circuit parameters
- Transmission line parameters
- S-Parameters
- Substrate effects

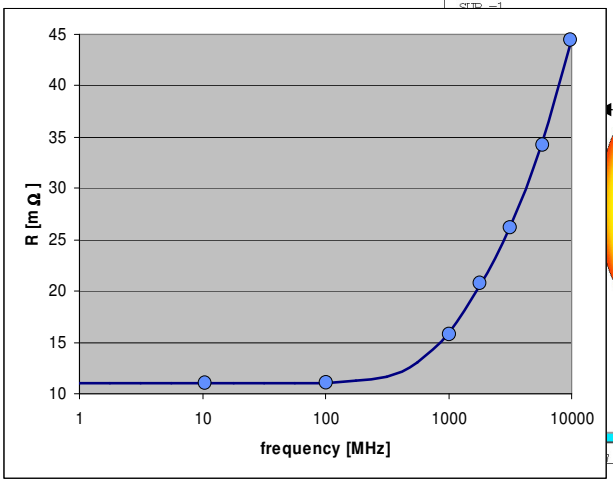
Solution

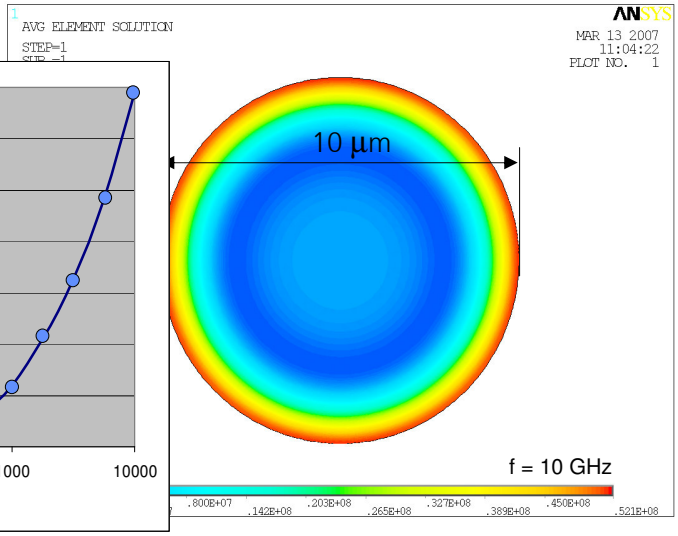
Mixture of tools and methods

- Analytical calculation
- Volume Filament Method (2D)
- ANSYS (2D and 3D)
- CST Microwave Studio (3D)

Electromagnetic analysis

Resistance and current density of single round via





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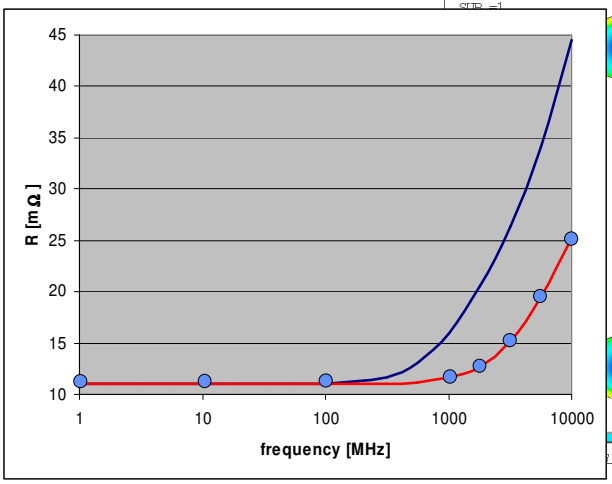
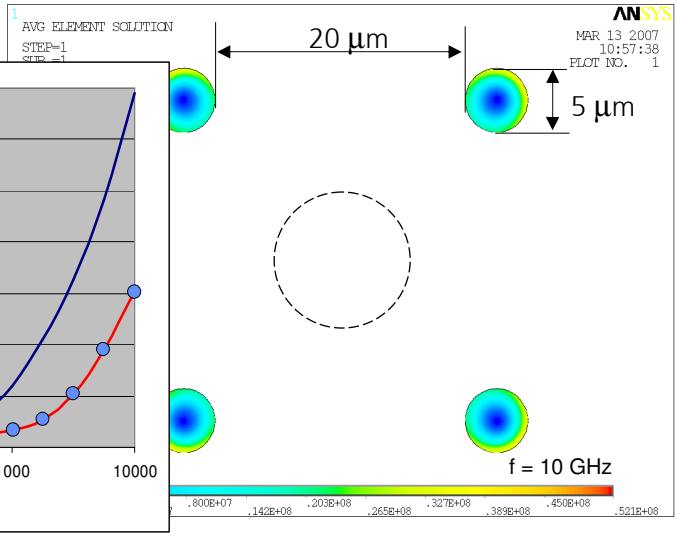
Electromagnetic analysis

Resistance and current density of via subdivided into four conductors





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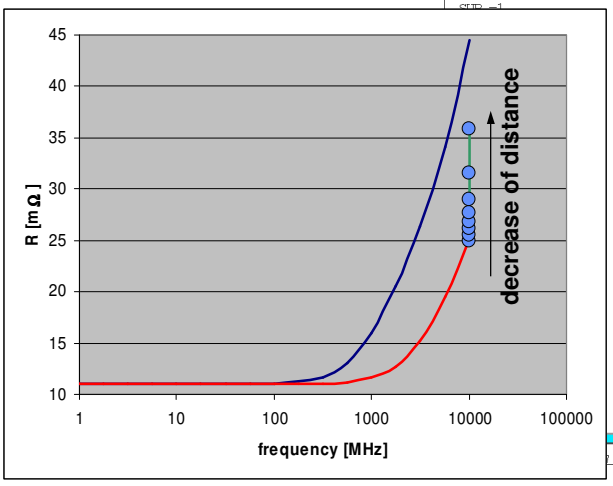
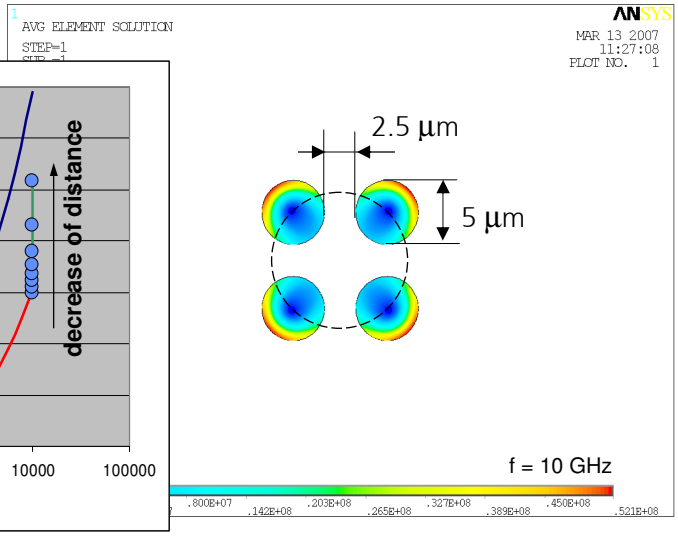
Electromagnetic analysis

Resistance and current density of subdivided vias and varying distance





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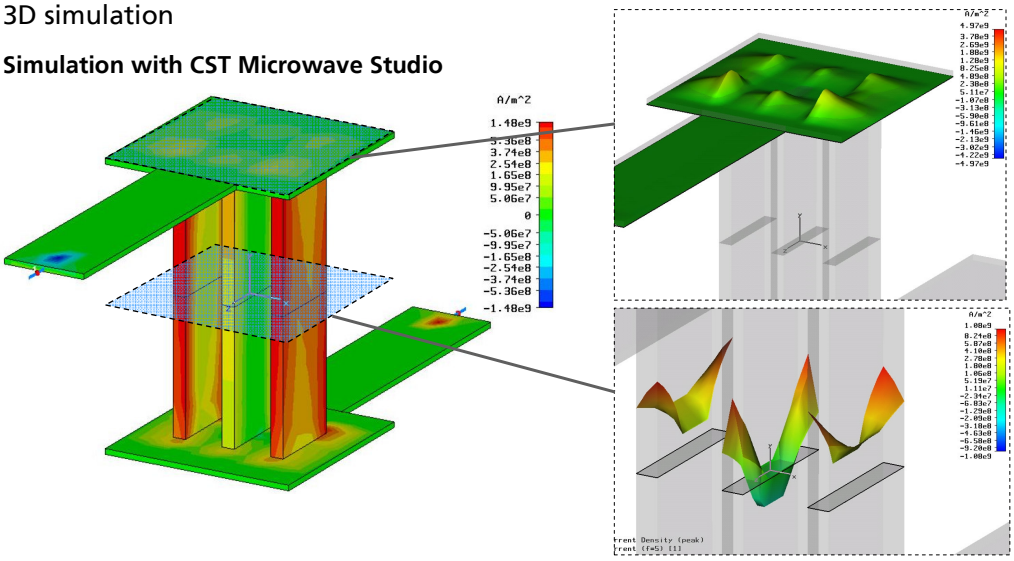
Electromagnetic analysis

3D simulation

Simulation with CST Microwave Studio



Current density in via structure

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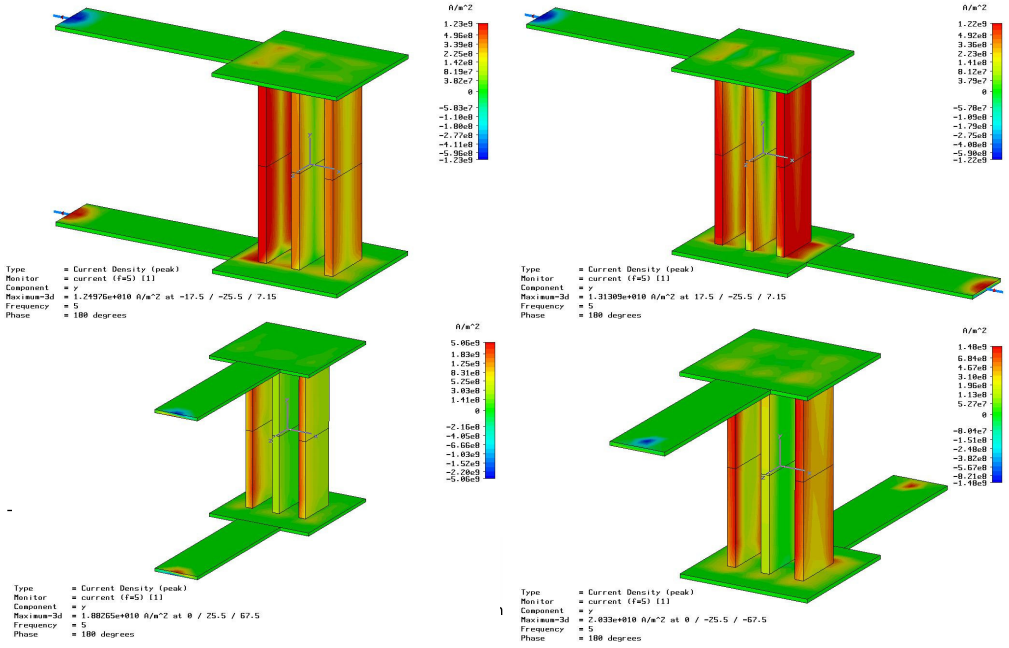
Electromagnetic analysis

3D simulation

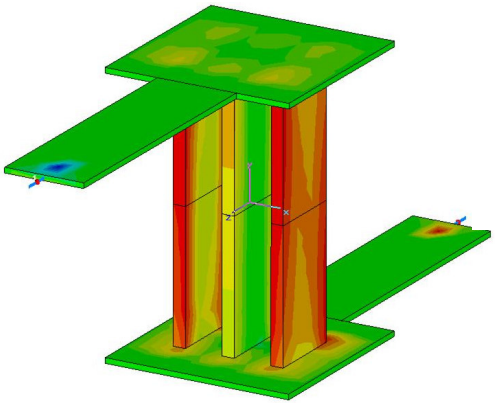
Simulation with CST Microwave Studio - Current density in via structures

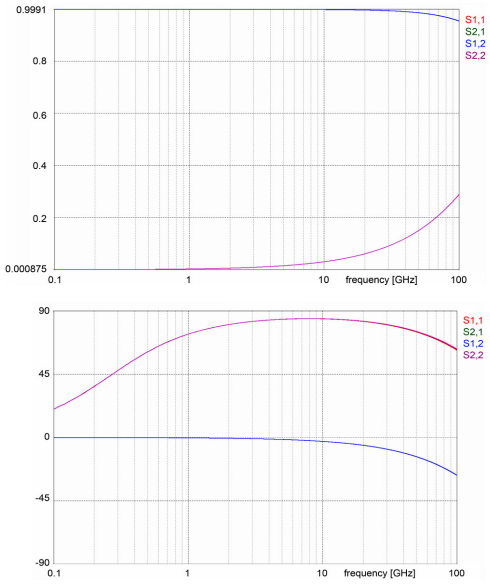


Electromagnetic analysis

3D simulation

Simulation with CST Microwave Studio





S Parameters of via structure

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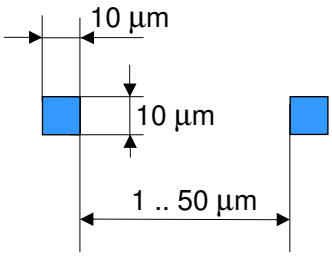
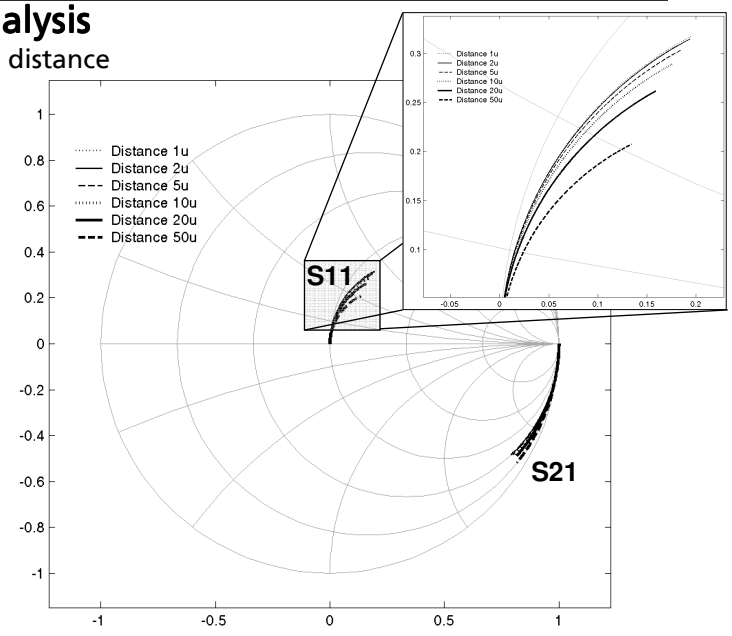
Electromagnetic analysis

S Parameter for varying via distance

Tungsten via structure





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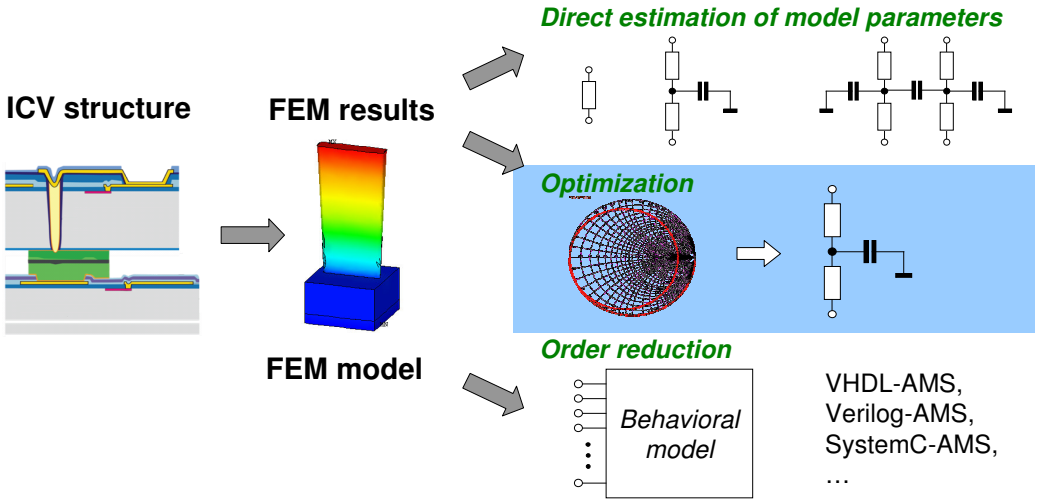
System level modeling



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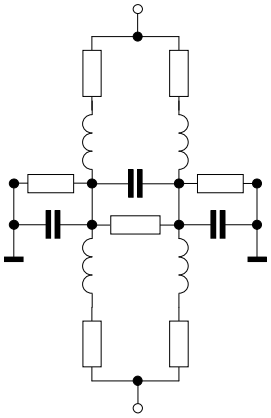
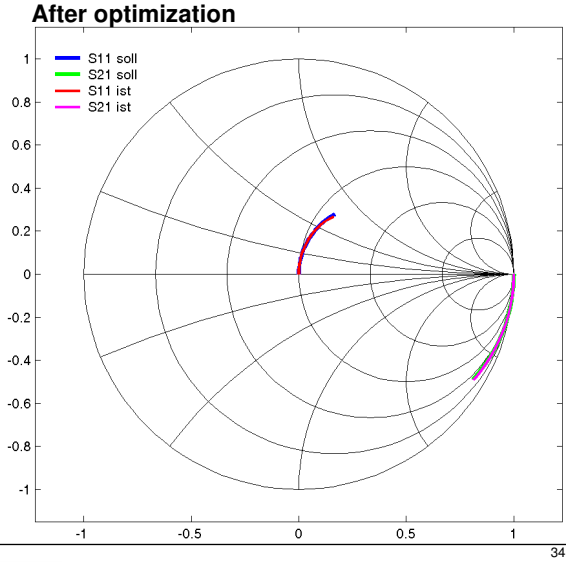
Electromagnetic analysis

Adaptation of circuit parameters by optimization algorithms

Network model



After optimization



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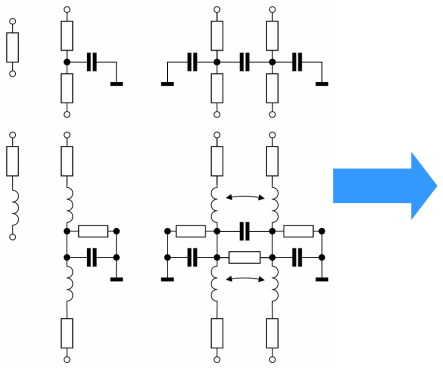
Outline

- Introduction
- Methodology for multi-level and multi-physics analysis of interconnect structures
- 3D Integration process based on ICV-SLID
- Thermal analysis and electro thermal simulation
- Modeling of electrical behavior at low and high frequencies
- **Design flow integration and system level simulation**
- Conclusions

Design Flow Integration

Analog and mixed-signal simulation

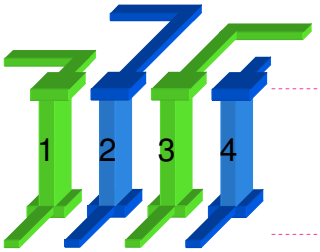
- SPICE netlists
- Behavioral models (VHDL-AMS, Verilog-AMS)

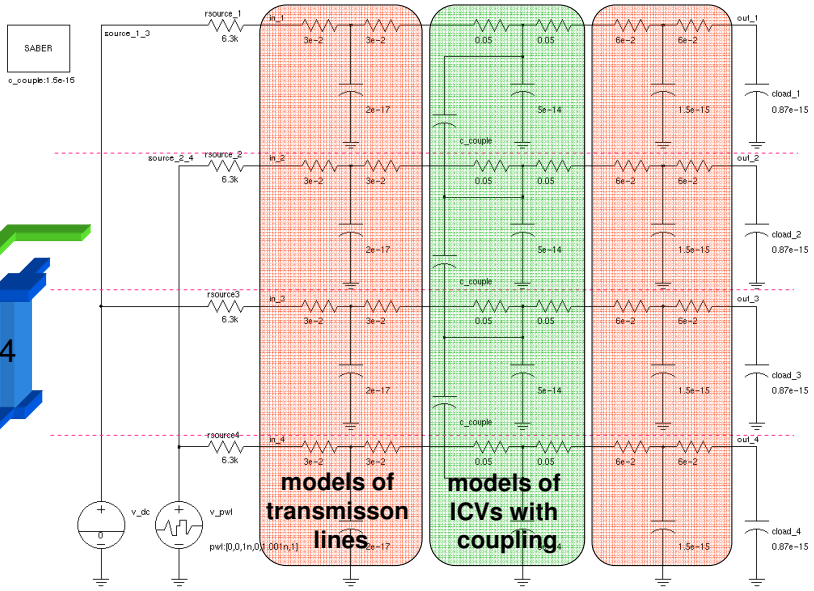


```
* subcircuit for ICV
.subckt  SUB p1 p2
r11      p1       x1       3.509906740674958e-02
l11      x1       x2       7.303141078165223e-11
r12      x2       x3       3.509906740674958e-02
l12      x3       p2       7.303141078165223e-11
r13      p1       x4       3.509906740674958e-02
l13      x4       x5       7.303141078165223e-11
r14      x5       x6       3.509906740674958e-02
l14      x6       p2       7.303141078165223e-11

c2       x2       0        5.605719883013937e-15
r2       x2       0        6.937740789761995e+05

c3       x5       0        1.089087152822265e-15
r3       x5       0        9.476916549535635e+05

c4       x2       x5       6.541443292856858e-23
r4       x2       x5       8.420367579889181e+07
.ends
```

System level modeling – crosstalk simulation

4 coupled ICVs





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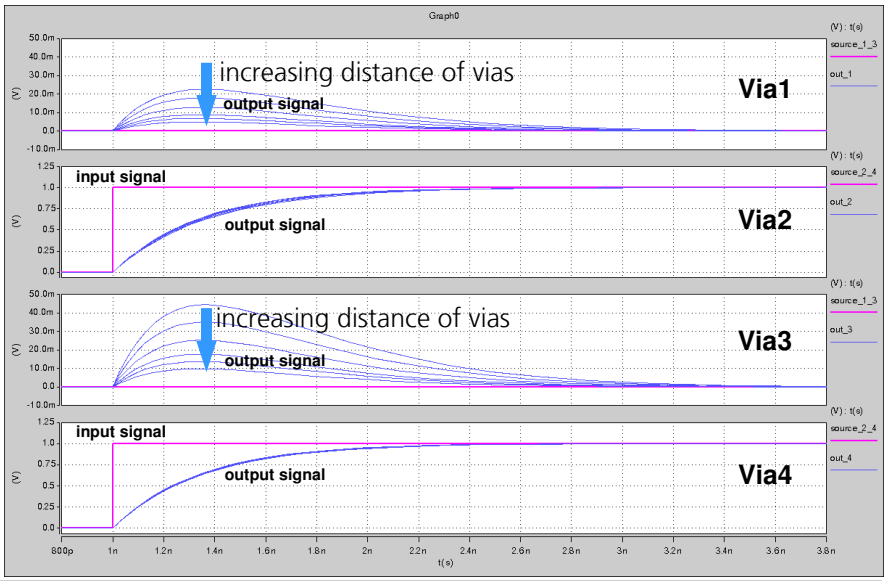
System level modeling – crosstalk simulation

crosstalk
2->1

crosstalk
2 ->3<-4



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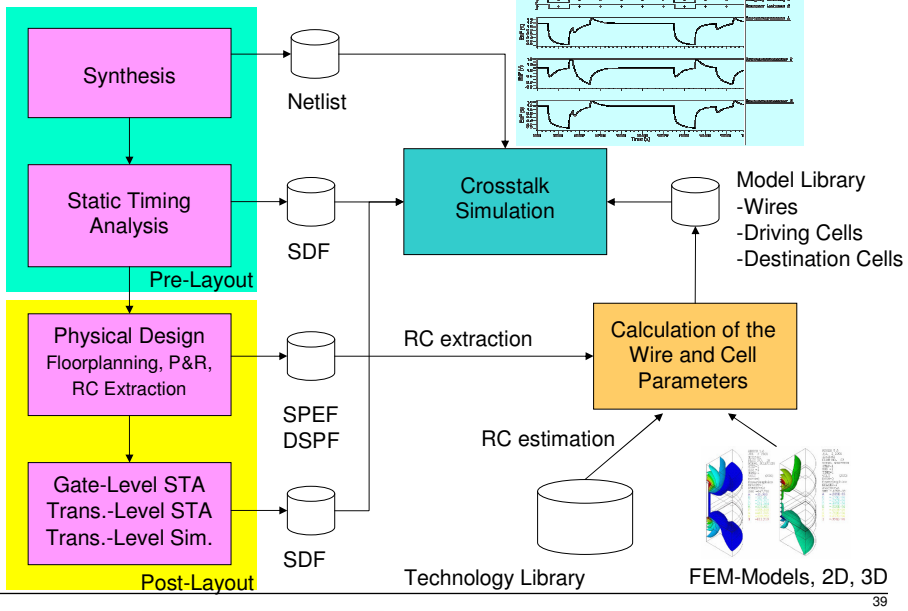
Design Flow Integration



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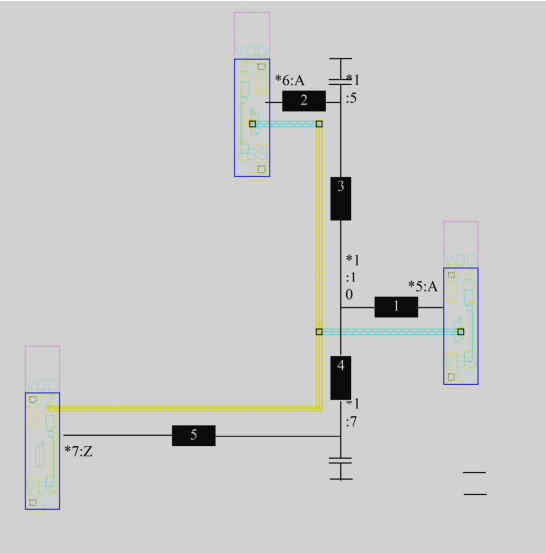
Design Flow Integration

Standard Parasitics Exchange Format – Layout structure and SPEF file




```
*SPEF "IEEE 1481-1999"
*DESIGN "o2"
*DATE "Mon Aug 20 12:23:31 2007"
*VENDOR "Synopsys"
*PROGRAM "Star-RCXT"
*VERSION "2006.06                "
*DESIGN_FLOW "PIN_CAP NONE" "NAME_SCOPE
LOCAL"
*DIVIDER /
*DELIMITER :
*BUS_DELIMITER []
*T_UNIT 1.00000 NS
*C_UNIT 1.00000 FF
*R_UNIT 1.00000 OHM
*L_UNIT 1.00000 HENRY

…

*CAP
1 *1:5  0.155816
2 *1:7  0.0210339
*RES
1 *5:A  *1:10 6.17814
2 *6:A  *1:5  1.85000
3 *1:5  *1:10 8.3476189
4 *1:10 *1:7  0.0691947
5 *7:Z  *1:7  7.25068
*END
```

Design Flow Integration

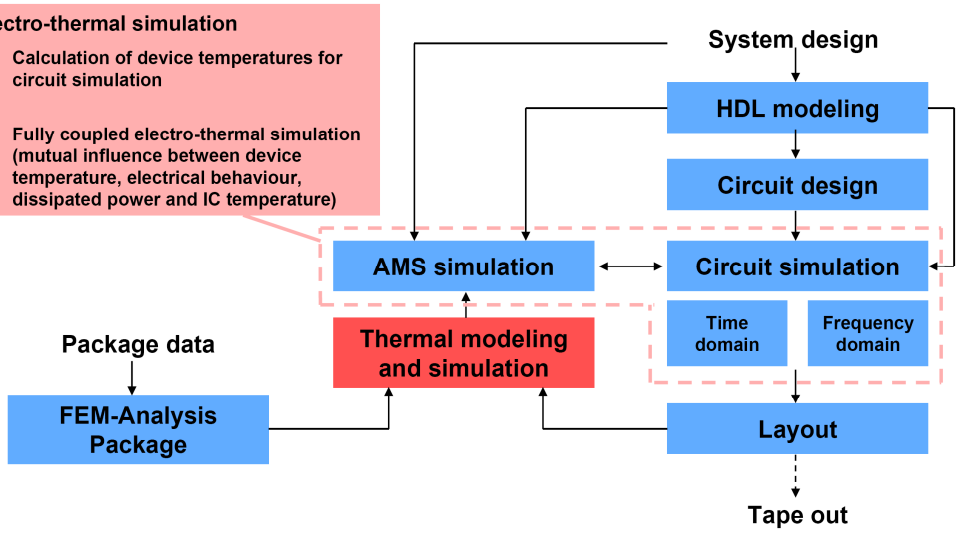
Electro-thermal simulation

Electro-thermal simulation

1. Calculation of device temperatures for circuit simulation

or

2. Fully coupled electro-thermal simulation (mutual influence between device temperature, electrical behaviour, dissipated power and IC temperature)



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Conclusions and outlook

Main challenges for design automation
- Multi-technology / multi-functional / multi-disciplinary / multi-physics
- handling of complexity by hierarchical modeling methodology

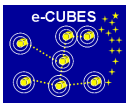
Knowledge about interconnect implementation
- is mandatory for robust design of actual system concepts
- enables the development of *new* system concepts and architectures

Development of manufacturing and design technology has to go hand in hand

Improvements in both technologies will be driven by applications

Acknowledgement

The presented work is partly based on



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