RELEVANT PINHOLE CHARACTERISATION METHODS FOR DIELECTRIC LAYERS FOR SILICON SOLAR CELLS

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ABSTRACT:
A wide range of dielectrics are used for photovoltaic (PV) applications (anti-reflection, passivation, insulation and masking layers) usually applied on large surfaces often presenting a texture or an important roughness. The application range of such a layer can heavily suffer from uncontrolled pinhole density. Therefore four pinhole characterization techniques have been compared regarding their relevance for current PV dielectric characterization. Two of these techniques present a good potential for the qualitative and quantitative pinhole characterization of especially for PV dielectric, on flat and rough surfaces. As a test for the characterization method an evaluation of the impact of aluminum evaporation on thick PECVD SiO_x pinhole density has been performed. This shows the ability of the characterization technique developed in this paper to perform quantitative pinhole characterization.

Keywords: Pinholes, plating, thin films.

1 INTRODUCTION

A wide range of dielectric layers is used in the photovoltaic (PV) industry; these layers are usually AntiReflective Coatings (ARC), passivation layers or insulating layers. For many of these applications, especially for advanced solar cell structures, a control of the pinhole density is essential.

A front contacting technique using electroless plating has been reported [1]. This technique uses the front ARC as a masking layer to define the front contact grid. Any open c-Si area, fingers and pinholes, is metalized during the Ni plating. This phenomenon (often called overplating, background plating or ghost-plating) induces areas of the wafer that are unwillingly plated. The reflectivity of the wafer can thus be increased by several percent.

Silicon surfaces covered by aluminum are highly recombinative, especially if no aluminum back surface field was formed. Therefore, pinholes in passivation layers expose locally the silicon surface to aluminum. This induces local recombination centers that increase the effective recombination velocity [2].

In certain advanced solar cell designs like rear-contact solar cells, base contact fingers can be separated from the emitter by a dielectric layer. Each pinhole in this dielectric would induce a local shunt reducing the solar cell performance [3].

The first step towards the understanding of pinhole formation is adequate characterization methods. In order to determine the factor influencing the pinhole density in photovoltaic processes, a characterization able to quantify the pinhole density on large rough surfaces is essential. Since polished surfaces are rarely used in the PV industry; the influence of the roughness on the pinhole density is worth taken into account.

Therefor different pinhole detection methods have been tried. One of them, developed in this work, aims to obtain accurate characterization of the pinhole density on large textured and non-textured surfaces.

2 EXPERiMENTAL

2.1 First characterization method: layer resistivity

The first characterization method uses the evaporation of an aluminum dot on top of the dielectric layer. Figure 1 shows the process flow that has been applied.

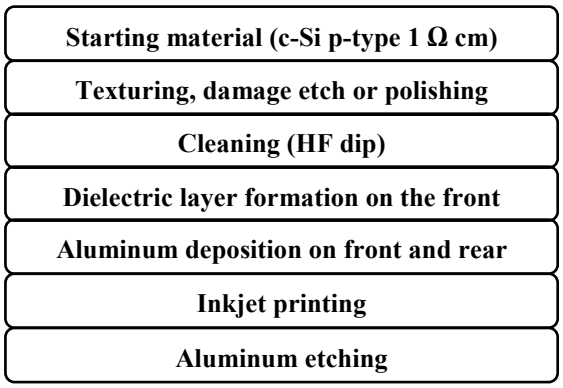


Figure 1: Process flow 1 used in the preparation of the samples for method 1. Our experiments were performed on Cz c-Si p-type 1 Ω cm wafers, on damage etched, ground and textured surfaces using either 100 nm PECVD SiO_x or 100 nm PECVD SiN_x as a dielectric layer.

After formation of the aluminum dot the measurement of the resistivity between the dot and the silicon has been performed. 1 V has been applied between the front and the rear contacts and the current has been measured by a picoamperemeter. The results obtained correspond to the resistivity of the dielectric layer. The resistivity of the layer decreases when the pinhole concentration increases. This characterization method is relatively quick but it is difficult to obtain a quantitative number concerning the pinhole density. This technique only leads to qualitative results.

2.2 Second characterization method: anisotopic etching

The second characterization technique is based on a chemical texturing of a silicon wafer coated with the dielectric layer [4]. When the substrate's crystal orientation is (100) an inverted pyramid, formed by an anisotropic basic etching of Si, appears below an etched pinhole. The samples are obtained following the process shown in Figure 2.

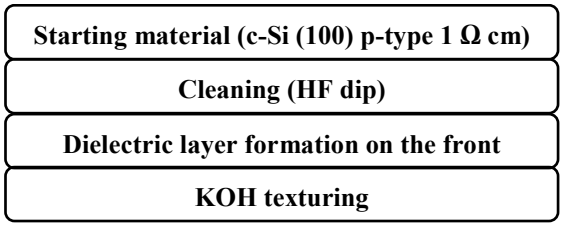


Figure 2: Process flow 2 used in the preparation of the samples for method 2. Our experiments were performed on Fz c-Si p-type 1 Ω cm wafers, on shiny etched surfaces using from 100 to 300 nm PECVD SiO_x as a dielectric layer.

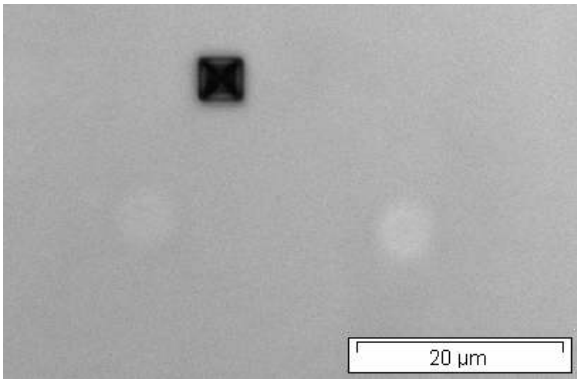


Figure 3: Microscopic picture of an inverted pyramid under a pinhole observed after applying process flow 2. Our experiments were performed on Fz c-Si p-type 1 Ω cm wafers, on shiny etched surfaces using 300 nm PECVD SiO_x as a dielectric layer.

When the pinholes are big enough the inverted pyramids can be detected and counted using a light microscope [4]. Figure 2 shows a light microscope picture of an inverted pyramid obtained following process flow 2.

This characterization presents the advantage that the samples are relatively simple to produce, however only large pinholes (~ 20 μm^2) can be detected through this method (see Figure 3). Small pinholes are difficult to observe with a conventional microscope. The small pinholes can be observed using a Scanning Electron Microscope (SEM) but this observation technique is on the other hand not well suited for pinhole counting on large areas (several cm^2). Furthermore, this method can not be applied to very rough or textured surfaces because the inverted pyramid become difficult to observe.

2.3 Third characterization method: Ni plating

The third detection method makes use of electroless nickel plating to coat the silicon in the pinholes in the dielectric layer. The Ni deposited on every Si surface in contact with the solution but the electroless nickel bath does not react with the dielectric areas. In our case only the pinholes were coated with Ni. Therefore the number of Ni dots formed corresponds to the number of pinholes. The sample preparation was performed applying the process flow shown in Figure 4.

The use of metal plating allows a selective deposition well suited for pinhole visualization. However Ni electroless plating alone is insufficient to observe the deposited metal with a standard microscope due to the small dot size. The SEM allows the observation of the Ni deposited on the pinhole (see Figure 5). However this observation technique is not well suited for pinhole counting on large surfaces.

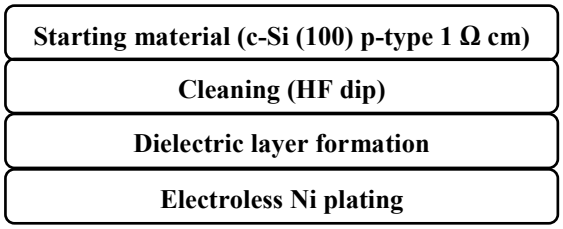


Figure 4: Process flow 3 used in the preparation of the samples for method 3. Our experiments were performed on Fz c-Si p-type 1 Ω cm wafers, on shiny etched surfaces using for 100 nm PECVD SiO_x as a dielectric layer.

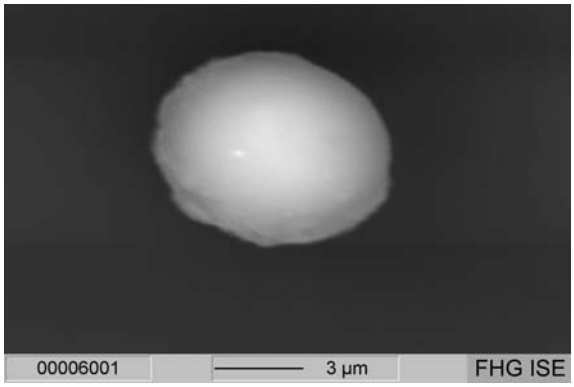


Figure 5: SEM picture of Ni dot on a pinhole. The sample has been obtained applying process flow 3. Our experiments were performed on Fz c-Si p-type 1 Ω cm wafers on shiny etched surfaces using for 100 nm PECVD SiO_x as a dielectric layer.

2.4 Fourth characterization method: Ni + Ag plating

The fourth pinhole characterization method has been developed at Fraunhofer ISE. A silver plating step is performed after the electroless plating of a seed metal layer of Ni on the pinhole [1, 5]. The silver can be thickened until a consequent diameter is reached. The Ag point is than easy to observe with a standard microscope. The excellent contrast with the coating due to the high reflectivity of the silver makes quantitative characterization possible even on KOH random pyramid textured surfaces. Figure 7 shows an Ag point above a pinhole obtained by this method. The substrate was KOH textured and covered with an ARC of silicon nitride (SiN_x).

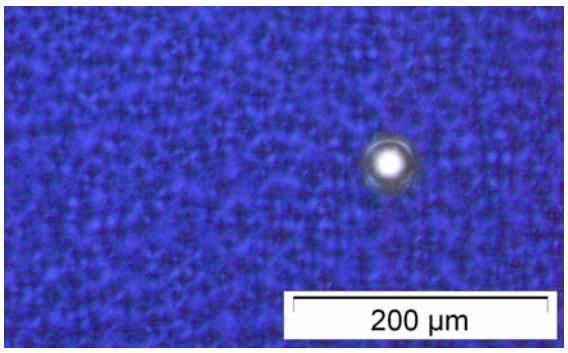


Figure 6: Microscopic picture of an Ag point. Our experiments were performed on Cz c-Si p-type 1 Ω cm wafers, on KOH textured surfaces using 70 nm SiN_x as a dielectric layer. The sample was obtained using the process flow 4.

Two techniques allow the deposition of Ag on the Ni seed metal layer, Light-Induced Plating (LIP) and ElectroPlating (EP). Figure 7 and Figure 8, respectively, show the process flow applied in order to produce samples suitable for Ag-LIP and Ag-EP.

Starting material (c-Si p-type 1 Ω cm)
Texturing, damage etch or polishing
n-type emitter diffusion
Back side emitter removal
Cleaning (HF dip)
Dielectric layer formation on the front
Back side aluminum deposition
Electroless Ni plating
Ag LIP

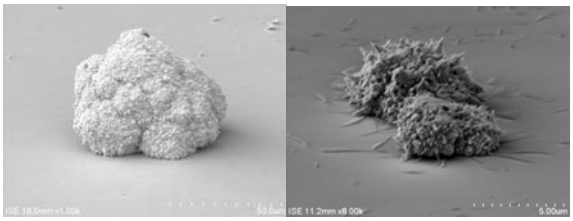
Figure 7: Process flow 4 used in the preparation of the samples for method 4. Our experiments were performed on Cz and Fz c-Si p-type 1 Ω cm wafers on shiny etched and textured surfaces using from 100 to 300 nm PECVD SiO_x as a dielectric layer.

Starting material (c-Si p-type 1 Ω cm)
Texturing, damage etch or polishing
Dielectric layer formation
Electroless Ni plating
Ag electroplating

Figure 8: Process flow 5 used in the preparation of the samples for method 4. Our experiments were performed on Fz c-Si p-type 1 Ω cm, on shiny etched wafers using 300 nm PECVD SiO_x as a dielectric layer.

The process flow 4 is more complex than the process flow 5. The quality of the silver deposition has been observed to be higher using LIP (process flow 4) than EP (process flow 5). However Ag points observable with a light microscope can be produced applying the process flow 4 and 5.

LIP provides an easy control of the current (light intensity) and a very homogeneous deposition over the wafer where EP often results in the formation of micelles (when the process cannot be controlled by limiting the current). Figure 9 shows Ag-plated points obtained using LIP and EP. The points obtained using LIP present a round compact shape whereas the points obtained using EP present picks that indicate the formation of micelles. The diameter of the Ag points can be controlled in both cases. For both techniques it is possible to observe the Ag point with a conventional microscope and to count them.



a) b)

Figure 9: SEM picture of an Ag dot obtained by LIP and EP. a) Ag dot obtained by LIP applying process flow 4, b) Ag dot obtained by EP applying process flow 5. Our experiments were performed on Fz c-Si p-type 1 Ω cm wafers, on shiny etched surfaces using 300 nm PECVD SiO_x as a dielectric layer.

In summary, the first pinhole characterization method and the fourth pinhole characterization method show the highest potential for qualitative and quantitative pinhole characterization, respectively, on large surfaces (several cm^2), planar or textured.

2.5 Example of application

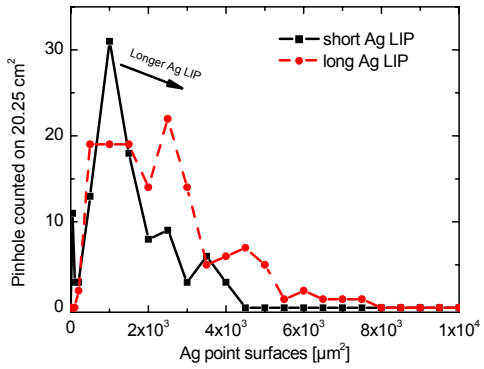
The influence of aluminum e-gun deposition on the pinhole density of thick plasma-enhanced chemical vapor deposited (PECVD) silicon oxide (SiO_x) layers was studied using the fourth characterization method as an example of application. The samples were prepared following the process flow 4. The starting substrates were shiny etched c-Si. 300 nm PECVD SiO_x was deposited (corresponding to process flow 4 step 6) after an HF dip. Two groups of wafers were processed:

- on the first group the Ni plating was performed directly after the SiO_x PECVD,
- on the second group the SiO_x PECVD has been deposited, than 2 µm aluminum was deposited on the SiO_x using e-gun, than the aluminum was etched by selective aluminum etching and only than the Ni plating was performed.

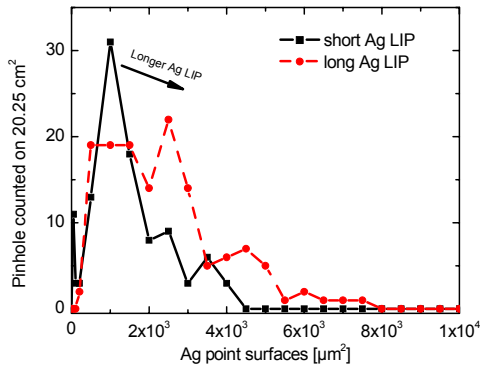
The Ag-LIP has been finally performed for the two groups of wafers.

Table I: Overall pinhole density

	short LIP	long LIP
SiO_x 300 nm	5.3 cm^{-2}	6.4 cm^{-2}
SiO_x 300 nm, Al evap. and etch.	12.8 cm^{-2}	15.5 cm^{-2}



a)



b)

Figure 10: Number of pinholes counted on an area of 20.25 cm^2 as a function of Ag point's surface. The sample has been obtained applying the process flow 4. Short and long LIP processes were performed. a) first group, b) second group. Groups are explained in the text above.

Figure 10 shows the number of pinholes automatically counted using light microscopy on an area of 20.25 cm^2 as a function of the Ag point's surface. Short and long Ag plating has been performed for the wafers of group 1 and 2. In order to quantify the error on the pinhole counting, counts have been performed also before Ag-LIP giving a result of 0 count on 20x25 cm^2. Moreover, we can observe that applying long Ag-LIP the surfaces of the Ag points increase. This test shows that the points that were counted correspond to pinholes. In fact if an Ag point surface is increasing with the plating time, this Ag point is necessarily in contact with the Si and therefore represents a pinhole.

Table I present the overall pinhole density counted by light microscopy for the wafer group 1 and 2. We observe that the pinhole density is low in both groups (~ 10 cm^{-2}). However, in the case where the samples were deposited with e-gun Al (2nd group) the pinhole density is more than two times higher than in the case where the samples were not deposited with e-gun Al (1st group). The observed pinhole density increase can be attributed to the aluminum evaporation itself or to the selective aluminum etching.

CONCLUSION

A comparison of four different pinhole characterization techniques applicable to current PV dielectrics is presented.

The first (dielectric resistivity measurement) and the fourth method (Ni and Ag plating) present an interesting potential for the qualitative and quantitative pinhole characterization of PV dielectrics on flat and textured large surfaces.

Thanks to the ability of method 4 a quantitative study evaluating of the impact of e-gun aluminum evaporation on pinhole density on thick PECVD SiOx was performed.

AKNOWLEDGEMENT

This work was supported by the European Union funded project „ULTIMATE“ under the project number ENERGY-2007-2.1-09-218966 .

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