Temperature Challenges for Integrated Systems due to High Power Density

ECPE Tutorial Wide-Bandgap User Training

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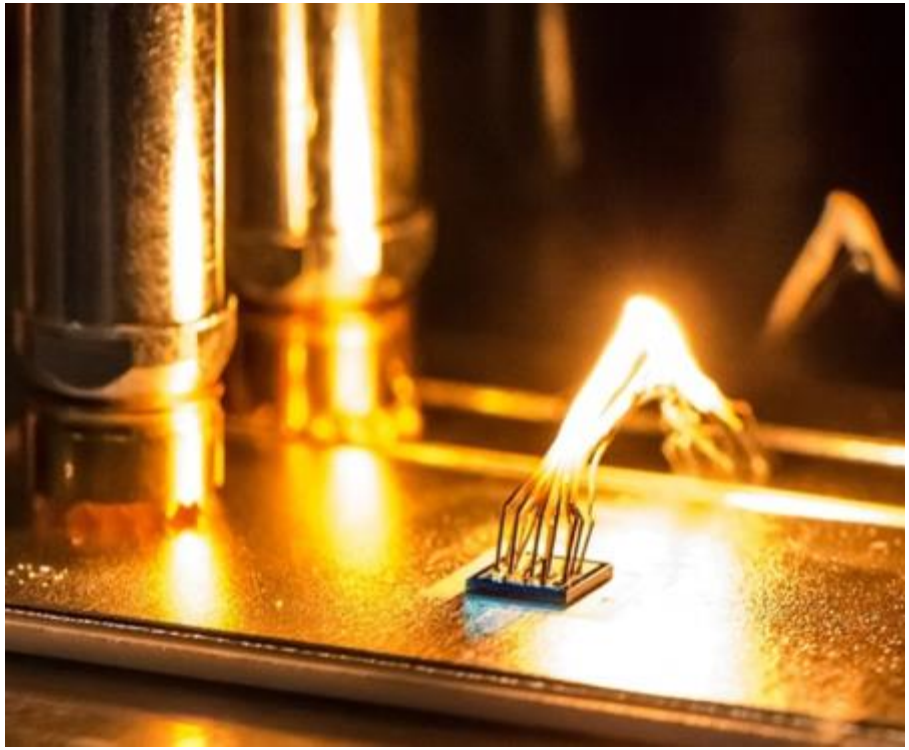

Picture source: Fraunhofer IISB

20.05.2021

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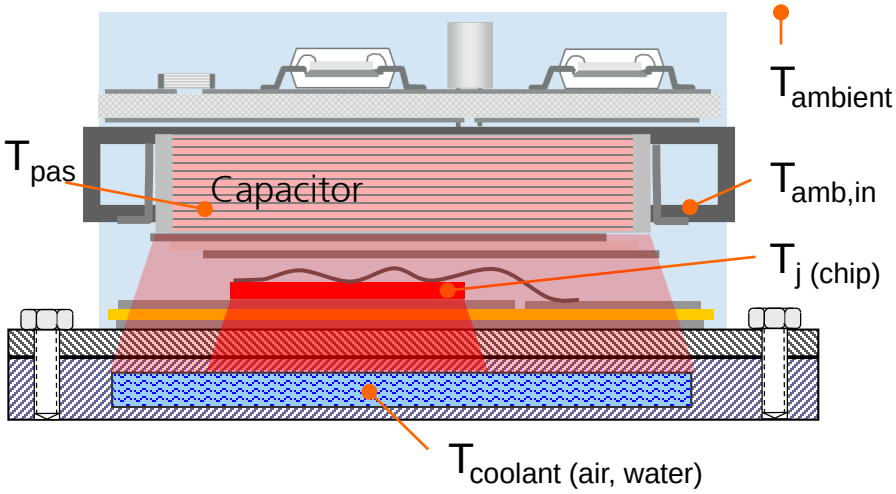
Contents

- Motivation
- Integration
  - Power Semiconductors
  - Passive components: DC-link capacitor
  - Electrical insulation
  - Die attach
- Conclusion



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Motivation

Take out advantage of high speed switching
Power electronics building block for easy use and cost reduction

Testability

Integration

Many materials in one package → lifetime

High electrical field strengths

Smaller footprint – same functionality

Smaller devices

High current density

High power losses density

High temperature

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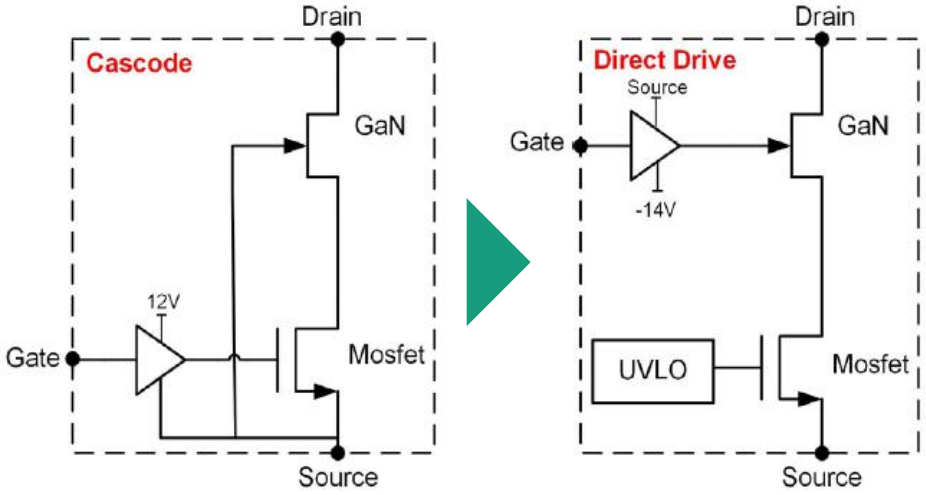
Integration Examples

- TI LMG3410
- QFN32 Direct drive concept
- Chip by Chip
- 600V/ 12A/ 70mΩ
- Chip Size GaN
  2.1mm x 5.7mm=11.97mm²
- Chip Size Si
  1.3mmx2.7mm=3.51mm²
- All functionality integrated into Si
- State of the art reflow soldering
- Temp max. 150°C



Paul L. Brohlin et.al.: The benefits of direct drive for GaN devices are achieving high switching power efficiencies and better system level reliability due to the integration of device protections, Texas Instruments;Texas Instruments LMG3410 Datasheet

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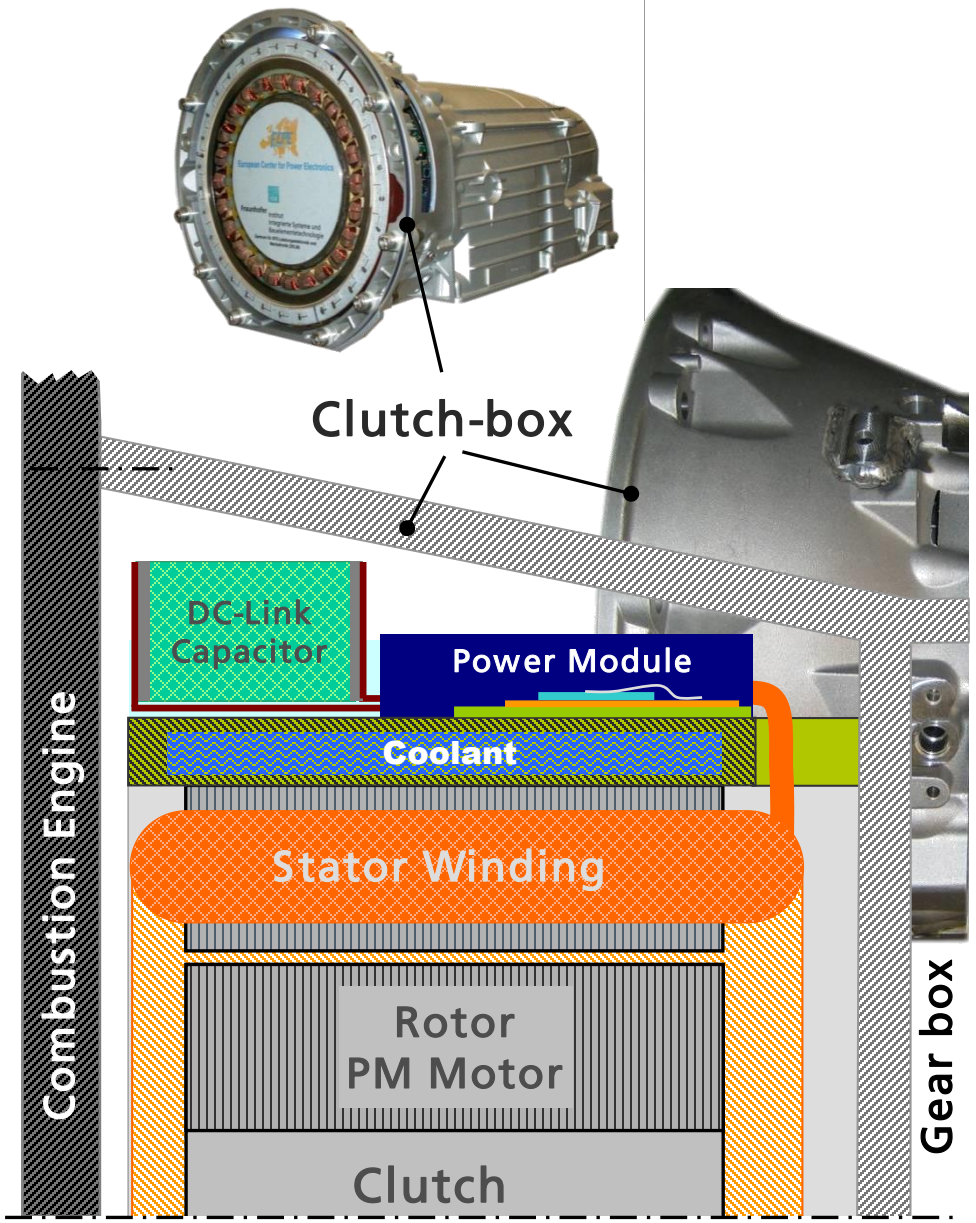
What's Integration?
Integration Examples

System integration

- Electric motor
- Cooling channel
- 3x Halfbridge power modules
- 3x Halfbridge gate drivers
- 3x Current sensor
- 3x Thermal shielding
- Common dc link capacitor
- Control electronics
- EMI filter
- Housing against ambient



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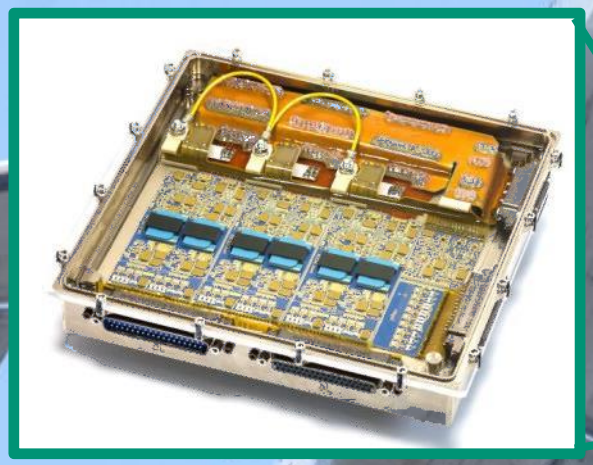
What's Integration? High Temperature



- Case Study:
  Research Project CREAM (EU)
  - DC/AC converter
  - Integrated with motor for a high temperature actuator
  - Assembled in multi-chip power module operated at 250°C junction temperature
  - SiC and SOI components
  - Output power: 7 kVA
  - Operating temperature range:
    -55°C / 170°C (cold plate)
  - Power density: 4.5 kW/liter for the demonstrator

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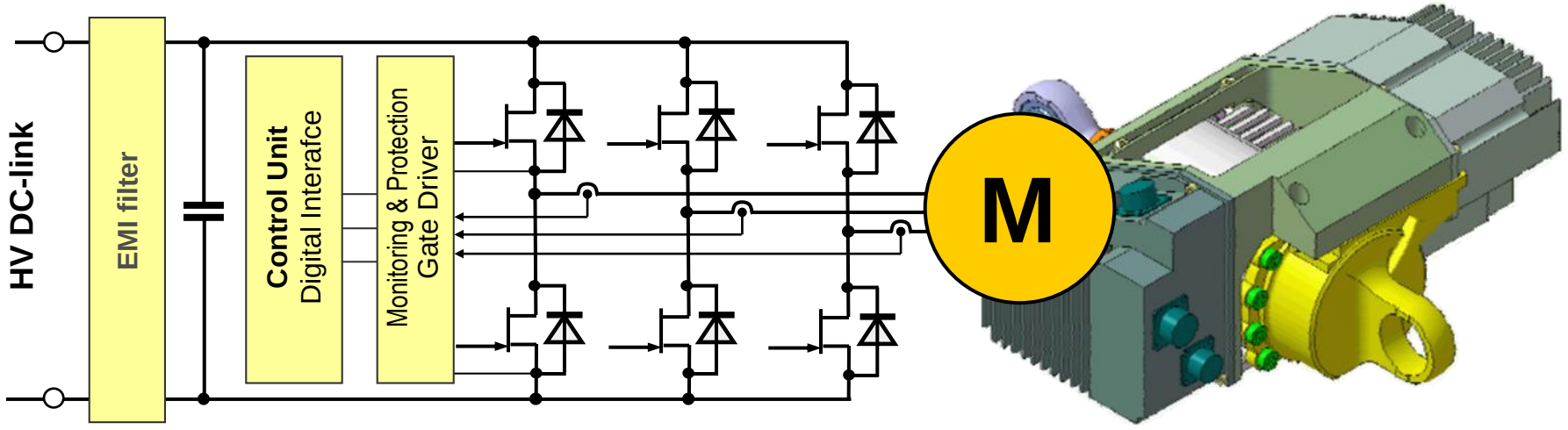
Power Electronics for High Temperature

- 6 Phase Inverter Bridge, SiC-JFET Half Bridge Power Modules
- Ceramic DC link capacitor
- Current Sensor for each motor phase
- Gate Driver with galvanic isolation via magnetics
- EMI Filter



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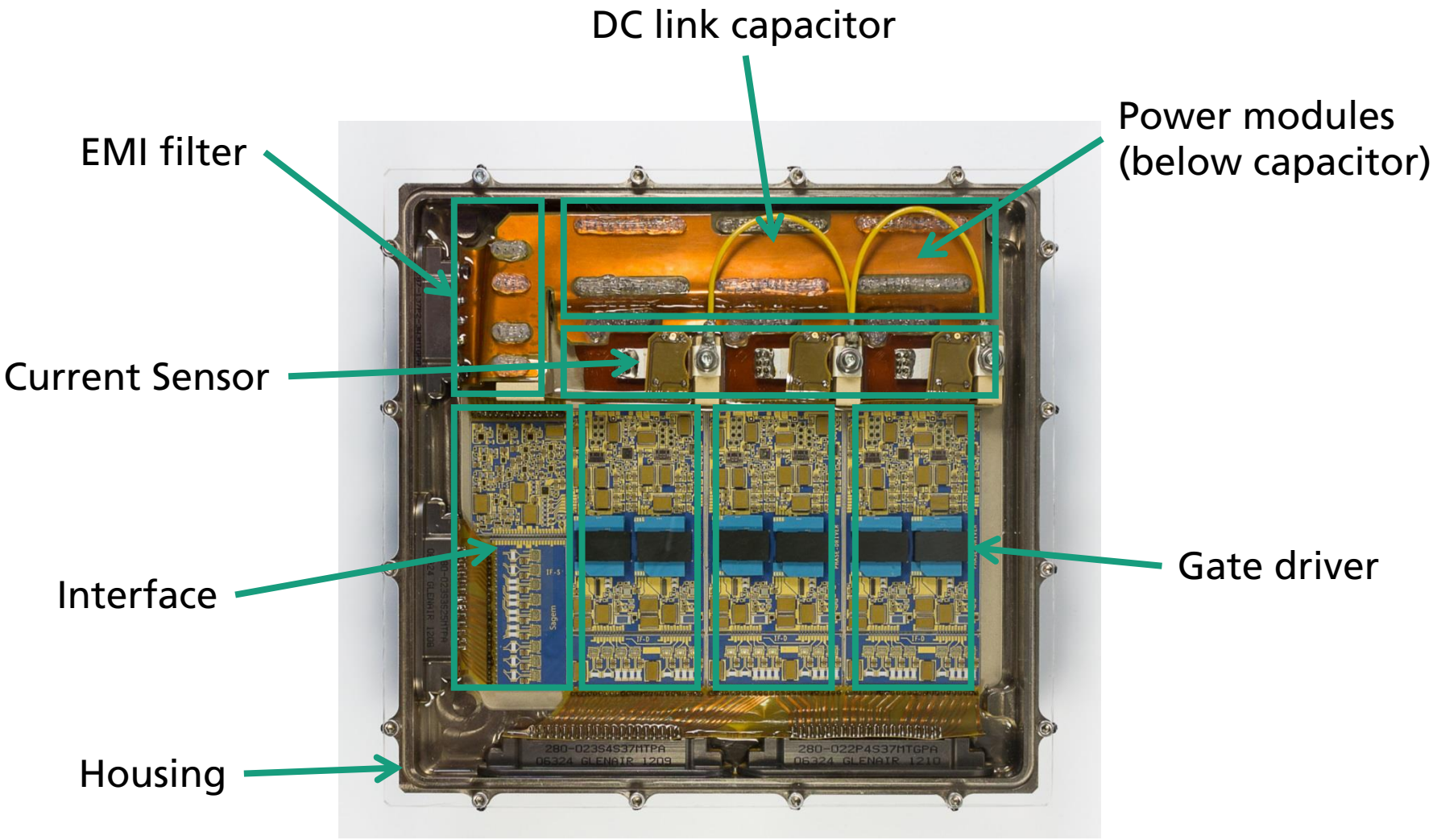
Power Electronics for High Temperature



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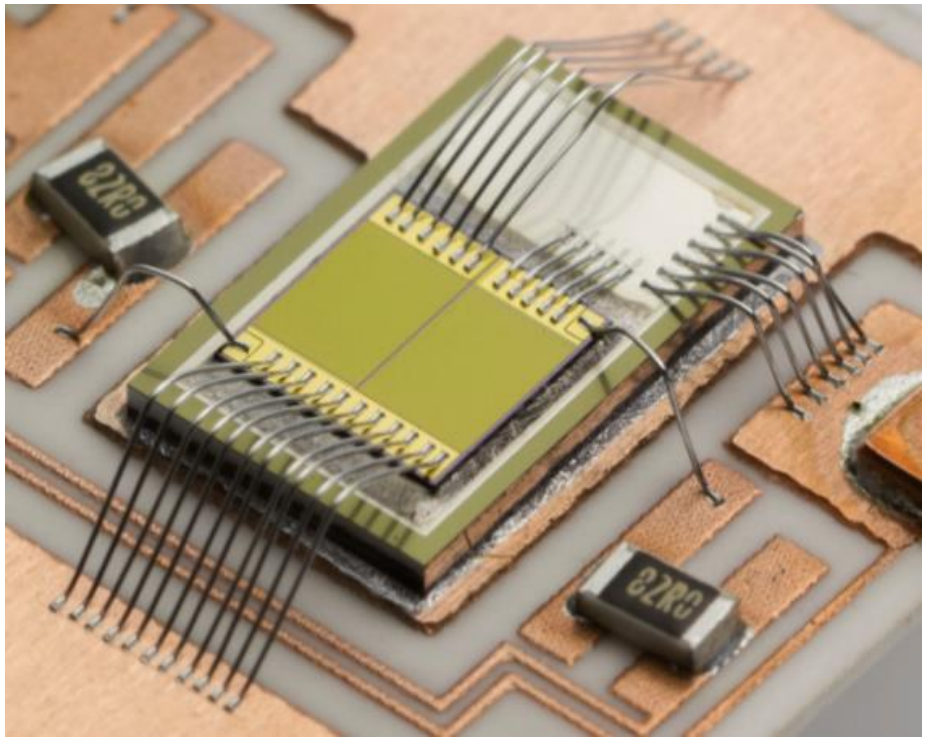
Integration Examples

- Monolithic GaN power stage
- Si dc link capacitor
- Die on Die concept
- Integrated gate driver
- Low parasitics
- Silver sintered die-attach for power devices
- Extended lifetime
- Temp …200°C



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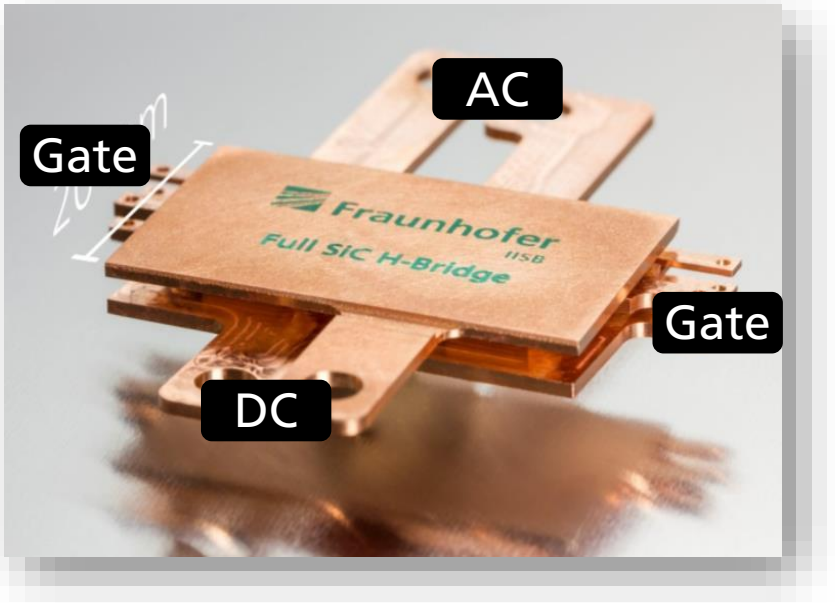
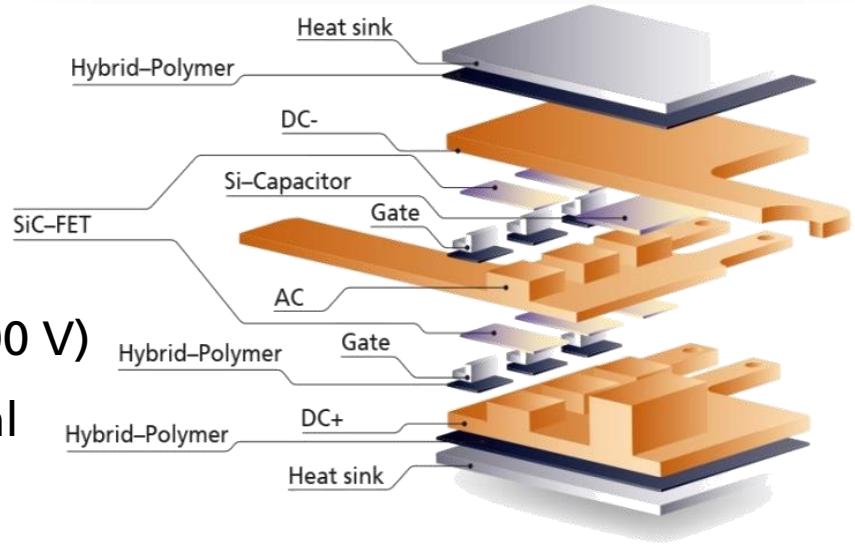
Integration Examples

- Concept
  - H bridge (600V/ 80A)
  - Chip on busbar
  - Minimal par. inductance < 2 nH
  - Operating temperature …250°C
- Technologies
  - Double sided Ag sintering
  - SiC MOSFET
  - Integrated Si-DC link capacitor (600 V)
  - Hybrid polymer insulation material





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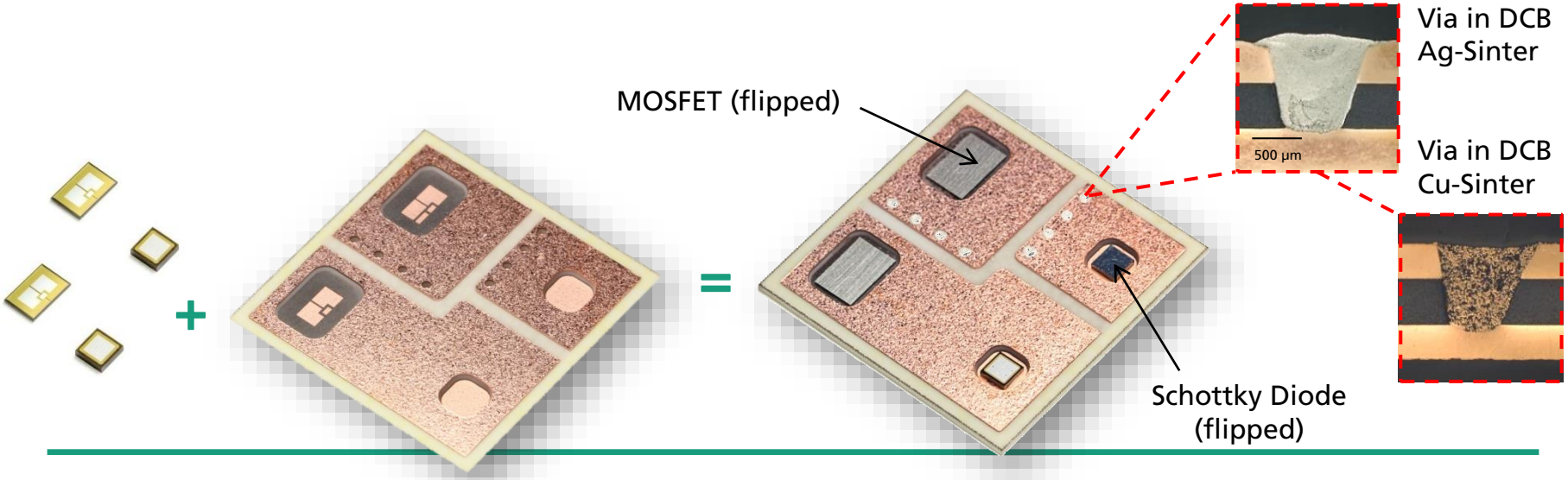
Integration Examples

Ceramic Embedding

- Goal: High temperature packaging for high voltage
- Problem: State of the art organic materials do not cover WBG needs
- Solution
  - Embedding in ceramic circuit board like DCB, LTCC
  - Subtractive laser ablation for extremely fine pitch and cavities



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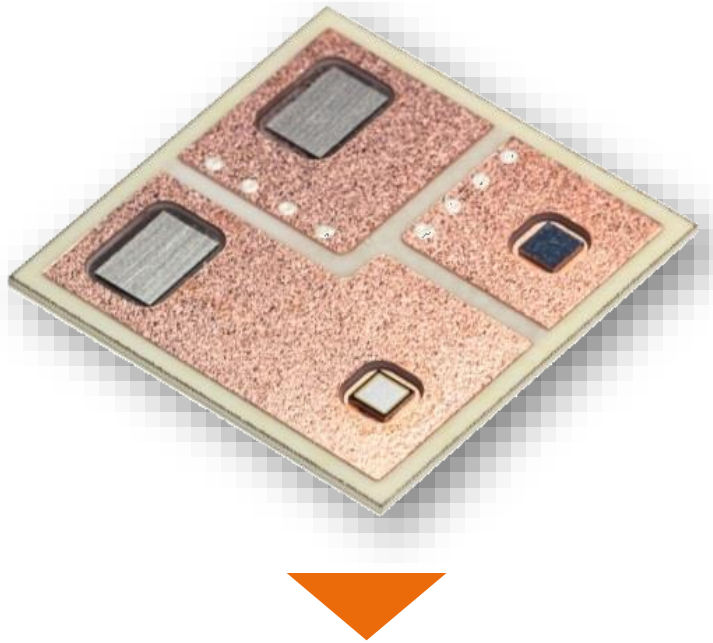
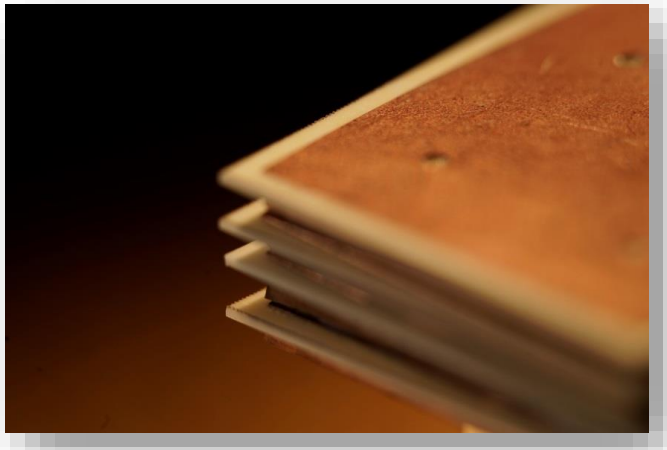
Integration Examples



Ceramic Embedding

- Highlights
  - High integration density
  - High temperature capability >300°C
  - High voltage resistant (>10 kV demonstrated)
  - Hermetic for harsh environments
- Relevance
  - Power electronics building block for air cooled applications



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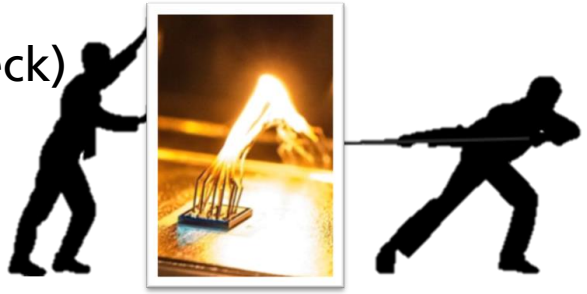
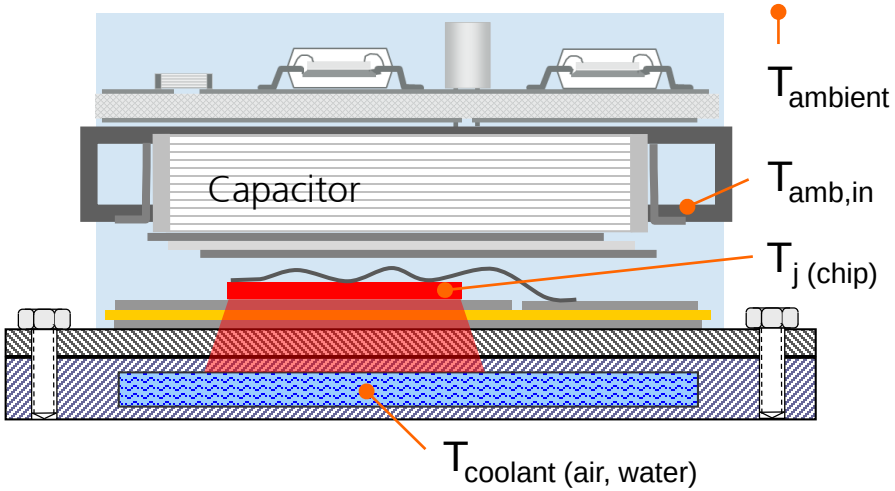
Integration Summary

- All components coupled thermally
- Technology push, two trends
  - Case A: Integration of power stage (GaN) and driver (Si, GaN), sensors (?), logic (Si), magnetics
    - Temperature keeps state of the art
    - First solutions on the market
  - Case B: Integration of power stage (SiC), dc link (Si, ceramic), parts of the gate drive
    - Temperature goes up (to the next bottleneck)
    - Demonstrated on power module level



Application Pull: Integration leads to High Temperature Power Electronics

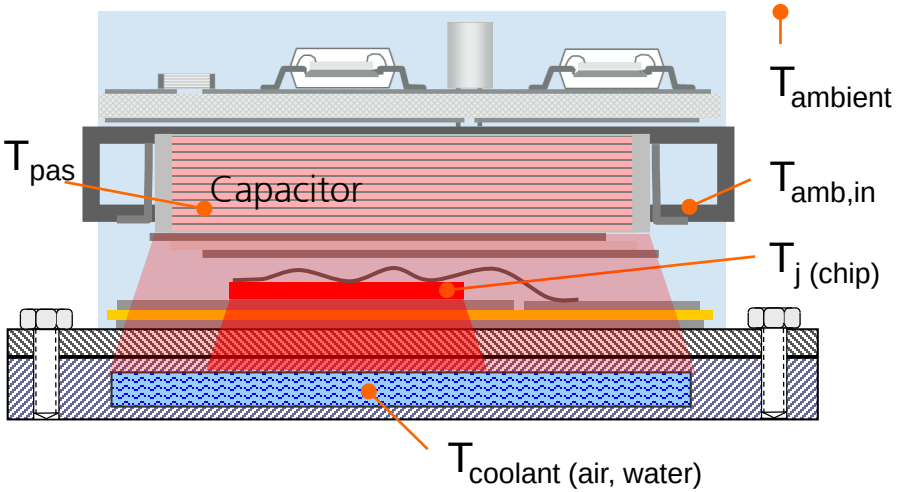
Case I



$T_{j(chip)} > 150°C$ ■ $T_{coolant,\ ambinent\_in} < 85°C$

- **Driver:** Low cost on semiconductor level
- **Challenge:** Only power semiconductor chip, its packaging and the heat path affected
- **Relevance:** Broad sustainable trend

Case II: SiC integration

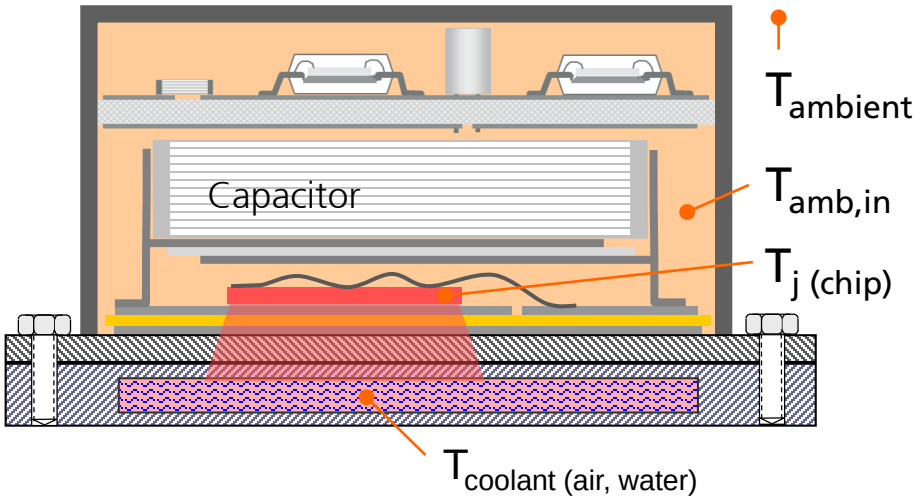


$T_{j(chip)} > 150°C$ ■ $T_{pas} > 85°C$ ■ $T_{cool,amb} < 85°C$

- **Driver:** Low cost and low volume for passives devices
- **Challenge:** Dielectrics, magnetics, packaging
- **Relevance:** Difficult but new capacitors available or on the horizon

Application Pull: Integration leads to High Temperature Power Electronics

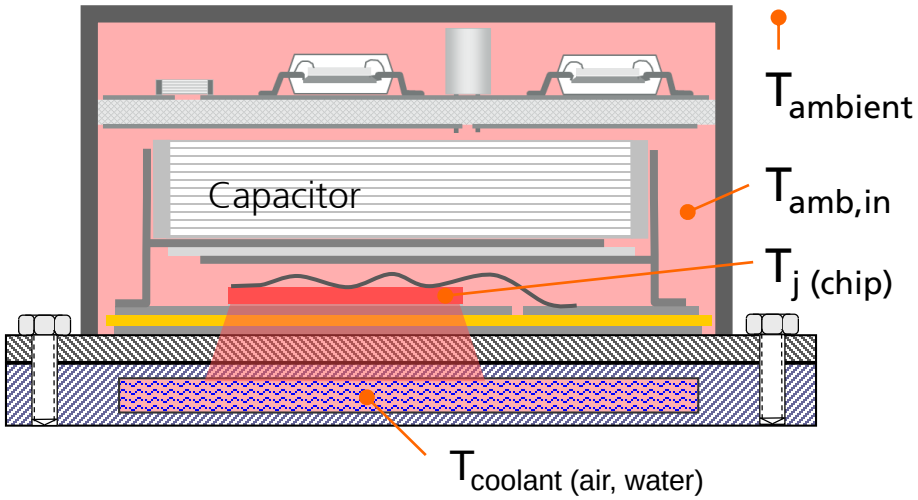
Case III



$T_{j(chip)}$ >150°C ■ $T_{cool,amb\_in,passives}$ = 85…125°C

- **Driver:** Low cost on system level*
- **Challenge:** All devices affected
- **Relevance:** Broad market but cost effective alternatives on system level available

Case IV: WBG full integration



$T_{j(chip)}$ >175°C ■ $T_{coolant,amb\_in,pasives}$ > 175°C

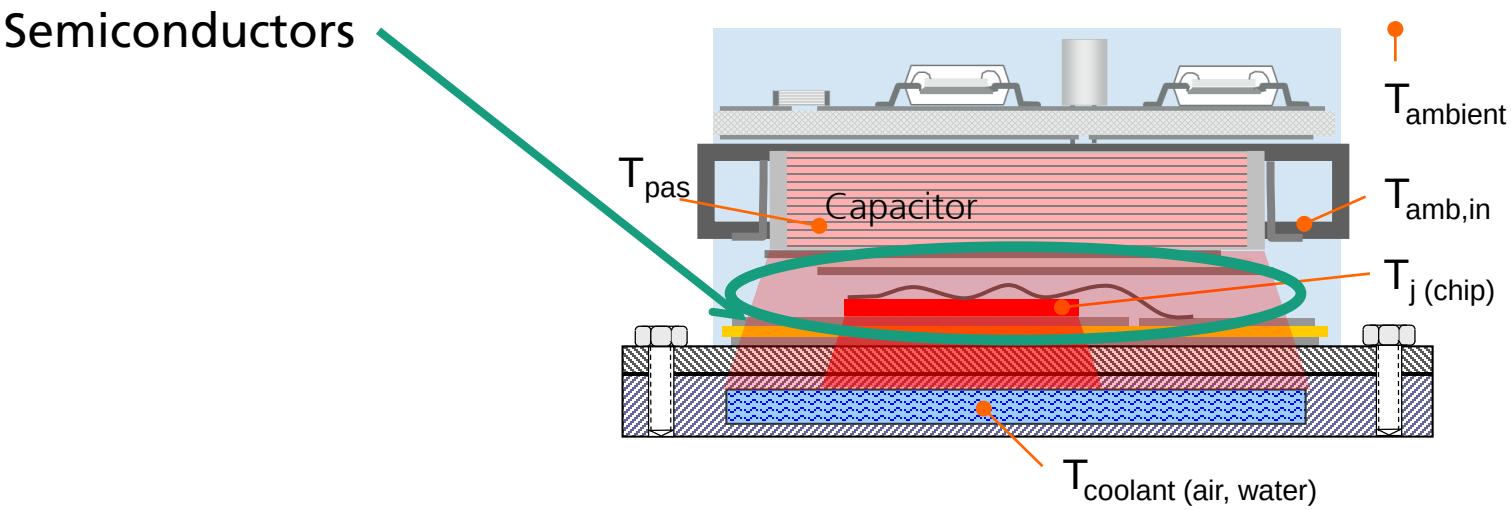
- **Driver:** Application needs**
- **Challenge:** All devices affected (availability, lifetime, cost)
- **Relevance:** Niche markets

* e.g. no second coolant ciruit for hybrid electric cars
** e.g. gear box electronics

Definition of High Temperature Power Electronics…

- …is strongly dependent on the application
  - High temperature power semiconductor
    - Reduces cooling effort, increases removable power losses
    - Reduces chip sizes and therefore cost
    - High temperature where beneficial
  - High temperature for the complete electronics
    - Reduces cooling effort
    - Makes it suitable for hot ambient
    - High temperature everywhere
    - Depending on the temperature
device by device and technology by technology
cannot keep up

Integration: Semiconductors



Technology Push: Semiconductor Devices (1)

Material	Bandgap energy, E_g in eV	Intrinsic carrier conc., n_i in cm^{-3}	Permeability ε_r	Electron Mobility, μ_n in $cm^2/(Vs)$	Crit. el. field strength, E_c in MV/cm	Elec. sat. velocity, v_s in 10^7 cm/s	Therm. cond., λ in W/(cmK)	Bandgap type
Ge	0.66	2.4E13	16.0	3900	0.1	0.5	0.6	I
Si	1.1	1.5E10	11.8	1350	0.3	1.0	1.5	I
GaAs	1.4	1.8E6	12.8	8500	0.4	2.0	0.5	D
InN	1.86	~1E3	9.6	3000	1.0	2.5	-	D
Al_5Ga_4As	1.9	-		3000	0.3		0.1	
GaP	2.3	7.7E-1	11.1	350	1.3	1.4	0.8	I
SiC (6H)	2.9	-	9.7	415	2.5	2	5	I
SiC (4H)	3.26	8.2E-9	10	~700	2.0	2.0	4.5	I
GaN	3.39	1.9E-10	9.0	900	3.3	2.5	1.3	D
Ga_2O_3	4.8	-						
C	5.45	1.6E-27	5.5	1900	5.6	2.7	20	I
Diamond	5.6	-	5.7	4000	10	3	20	I
BN	6.0	1.6E-31	7.1	5	10	1.0	13	I
AlN	6.1	~1E-31	8.7	110	11.7	1.8	2.5	D

Ge…Germanium, Si…Silicon, GaAs…Gallium arsenide, InN…Indium nitride, $Al_xGa_{x-1}As$…Aluminum gallium arsenide, GaP…Gallium phosphide, SiC…Silicon carbide, GaN… Gallium nitride, Ga_2O_3…Gallium oxide, C…Carbon, BN…Boron nitride, AlN…Aluminum nitride

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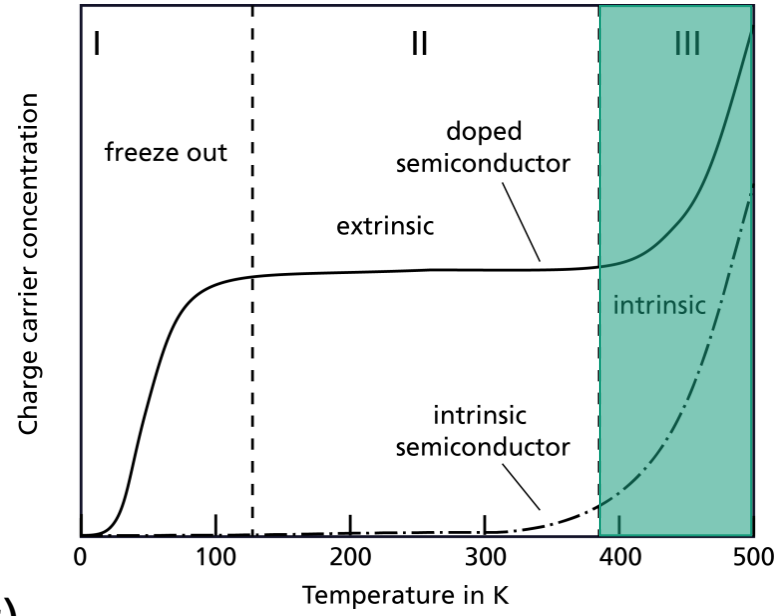
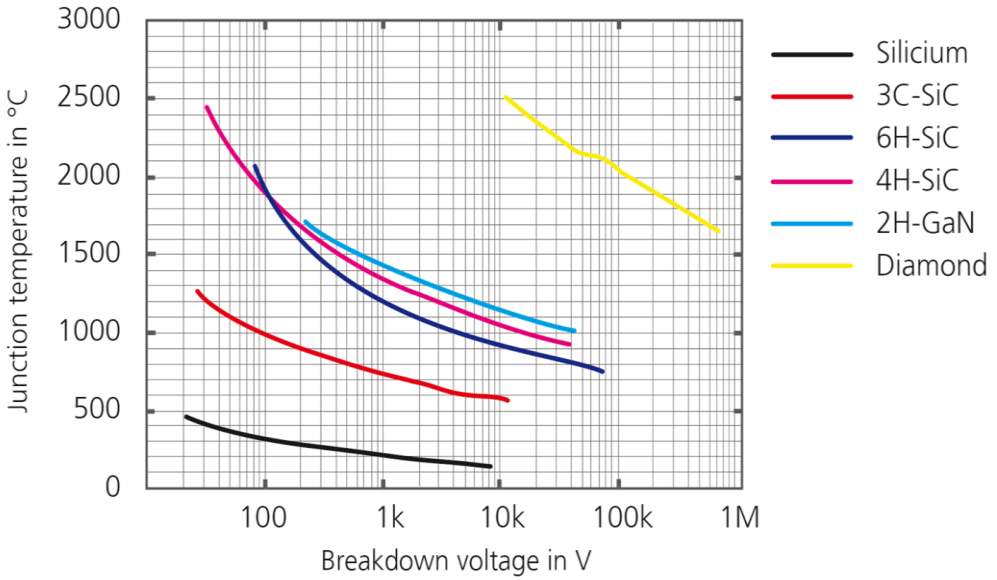
Technology Push: Semiconductor Devices
@ High Temperature

- With increasing temperature
  - Intrinsic vs. extrinsic @high T
  - increased reverse voltage
  - decreased forward voltage drops at pn junctions
  - decreased conductivities
  - increased gain in bipolar junction transistors (BJTs)
  - decreased threshold voltages in field effect semiconductor transistors (FETs)
  - Changed temperature coefficient
  - change in the switching characteristics, …



Technology Push: Semiconductor Devices

Thermal Runaway



- Power dissipation of a device increases with temperature (e.g. during blocking when leakage current causes heat up)
- The limits of thermal stability have to be taken into account when operating semiconductor devices
- The maximum operating temperature for semiconductors can be calculated from their intrinsic carrier density which depends on the band-gap of the material
- For HV applications the theoretical limit for Si devices is reached at 150 °C; for devices up to 100 V blocking it is supposed to be at 250 °C

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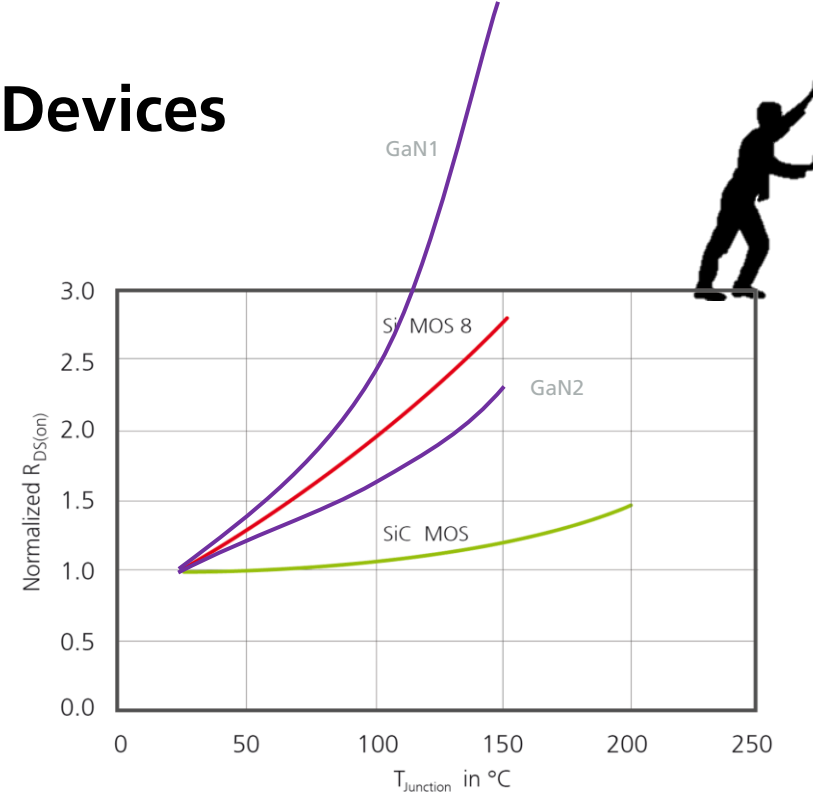
Technology Push: Semiconductor Devices
Electrical Properties of WBG

- Si 25..125°C: a factor of 2 is accepted by the application designers
- State of the art SiC on resistance increases by a factor of 1.5 at 200°C !
- SiC on resistance looks usable for high temperature
  → perfect candidate for dc-link integration
- GaN cannot keep up (so far)
  - Devices with a factor > 4 !
  - Devices available with a factor approx. 2 only
    → perfect candidate for driver & logic integration

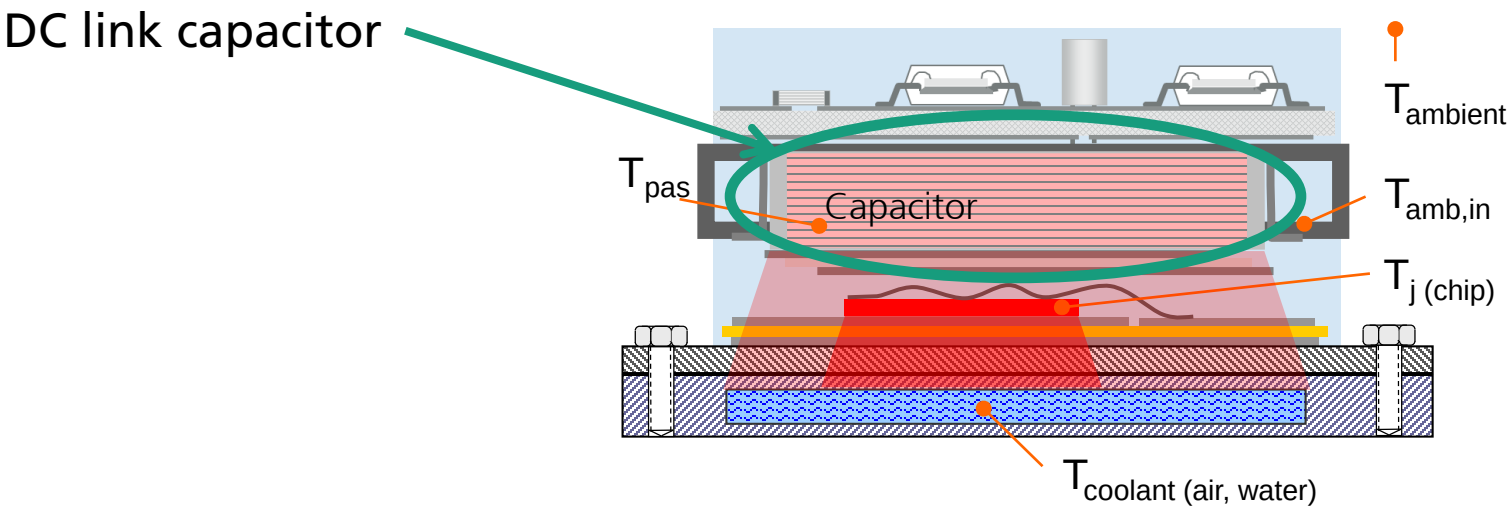


Comparison of the $R_{DS(on)}$
Si MOS8 (1.2 kV, 0.30 Ω Si MOSFET, Microsemi)
SiC MOS (1.2 kV, 80 mΩ SiC FET, Cree)
GaN1 FET (650V, 35mΩ, GaN FET, Transphorm)
GaN2 FET (600V, 140mΩ, GaN FET, Panasonic)

Technology Push: Semiconductor Dies (5)
Limits in High Temperature with Respect to the Device

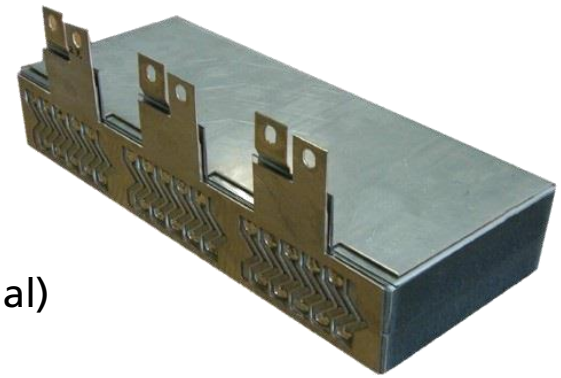
- Metallization of the device:
  - Ranging from up to 200 °C aluminum will satisfy almost all applications
  - From 200 °C the relatively low electro migration activation energy may need elements to suppress electro migration
  - More additives needed to further increase temperature to approx. 300 °C (simultaneously increasing resistivity of Al alloy)
  - > 300°C will afford copper or costly material (Au, Pt, …)
- Lifetime
  - High temperature swings degrade the metallization
  - High temperature degrade isolation (gate oxide)
- No real trend for temperatures > 200°C so far on the market

Integration: Passive components



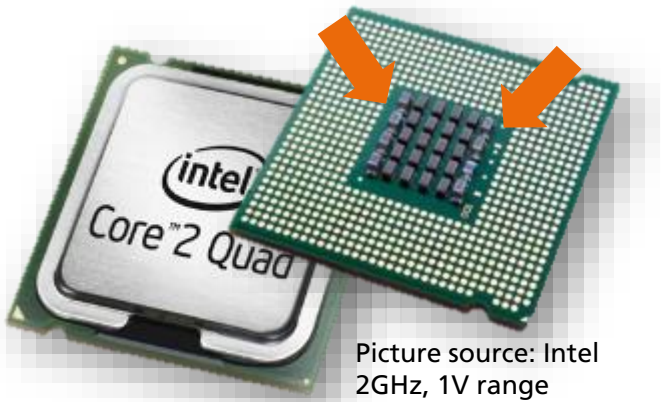
Technology Push: DC-link capacitors

- DC link capacitors for high temperatures
  - Electrolytic capacitors not suited
    - Simply too big
  - Foil capacitors go for 350°C with special material
    - Limited energy density
    - High power losses during operation (high temp material)
  - Ceramic capacitors
    - Big variety of different materials mostly based on BaTiO
    - Exciting energy densities available
    - Excellent high temperature capabilities
    - Candidate for integration
  - Silicon capacitors
    - Limited energy density
    - Exciting high power density
    - Excellent high temperature capabilities
    - Candidate for integration

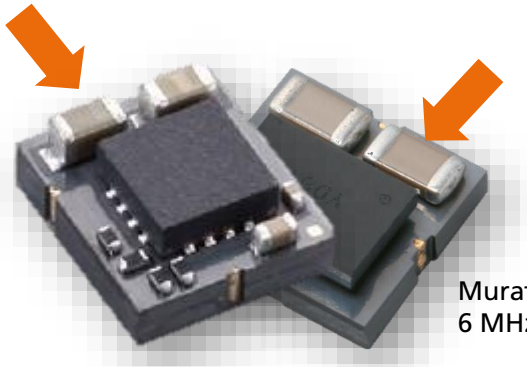


Technology Push: DC-link capacitors

- Nothing new!
- Well known from high performance micro processors…
- …and integrated DC/DC Converters for consumer electronics



Picture source: Intel
2GHz, 1V range



Murata LXDC,
6 MHz, 10V range

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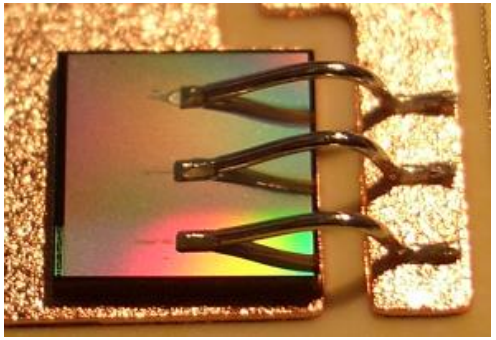
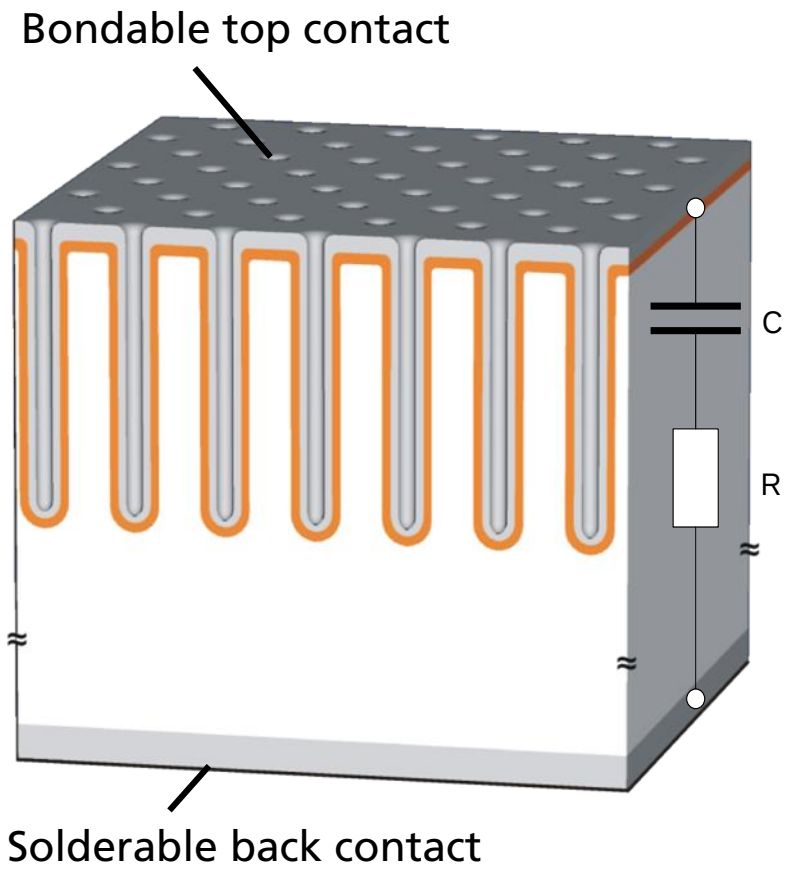
Technology Push:
Monolithic Integrated Silicon DC link Chip Capacitor

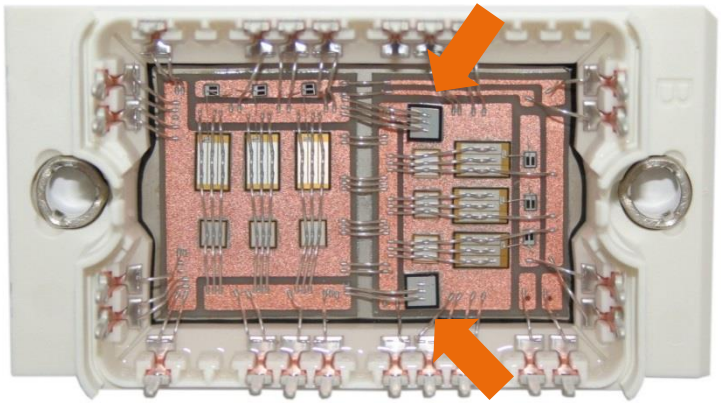
Device concept and implementation

- Integrated in silicon chip
- Voltage rating up to ~~600V~~ 900V
- Temperature rating up to 200°C
  Si is the substrate only, no semiconductor
- Capacitance: typ. 5-30nF
- Manufacturing of known technologies
- Packaging of known technologies

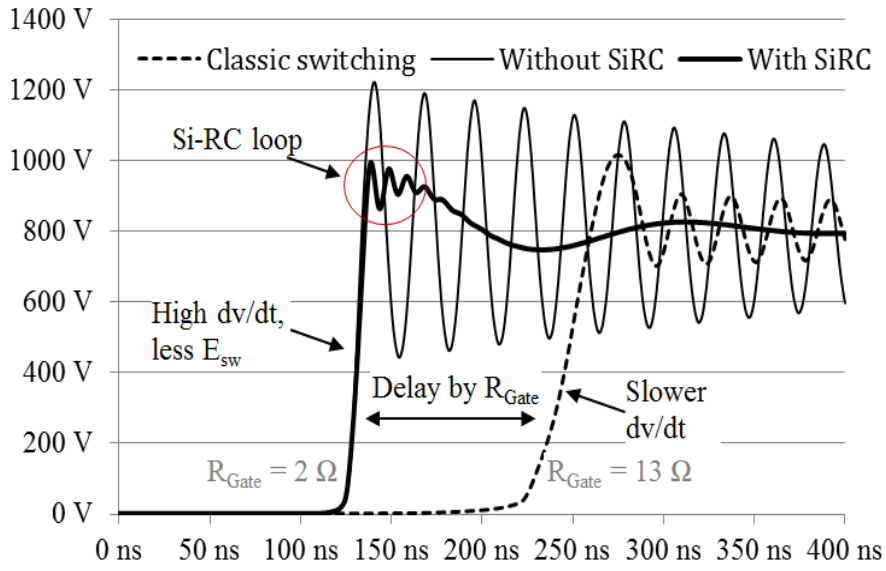


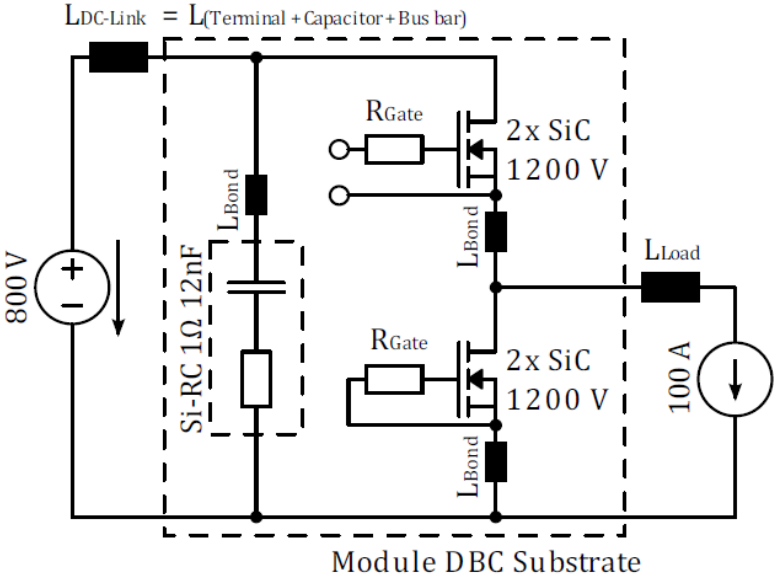


Technology Push:
DC Link Capacitors for Integration



- Comparison of switching methods
  - Classic slow (200V overshoot)
  - High speed (400V overshoot, -50% switching losses)
  - High speed with Snubber (200V overshoot, -50% switching losses!)





Matlok et. al, ECSCRM 2016

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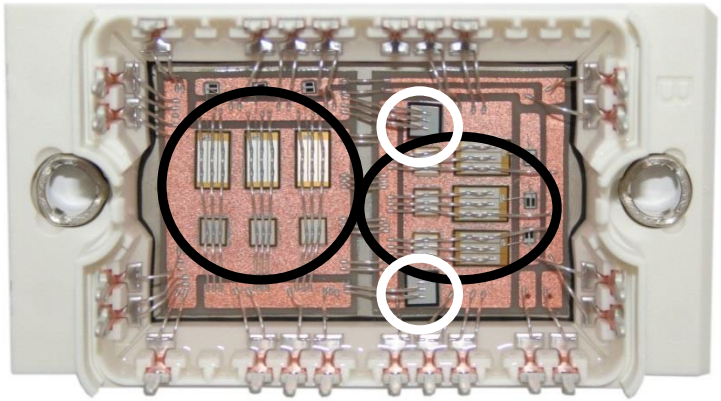
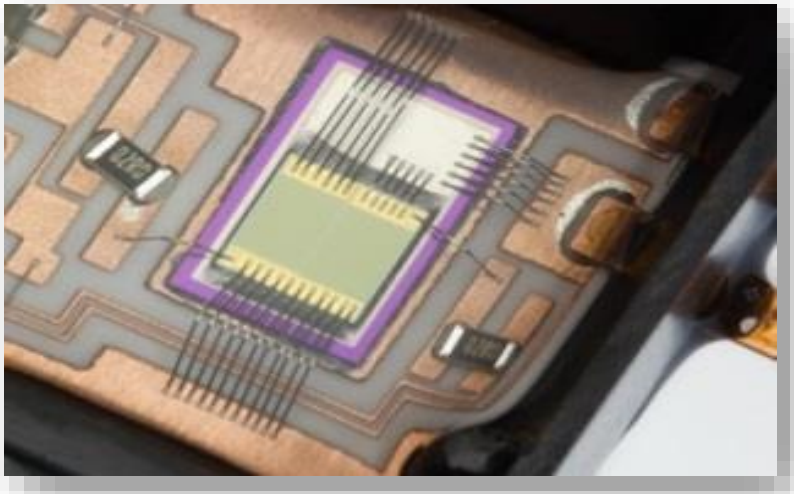
Technology Push:
DC Link Capacitors for Integration



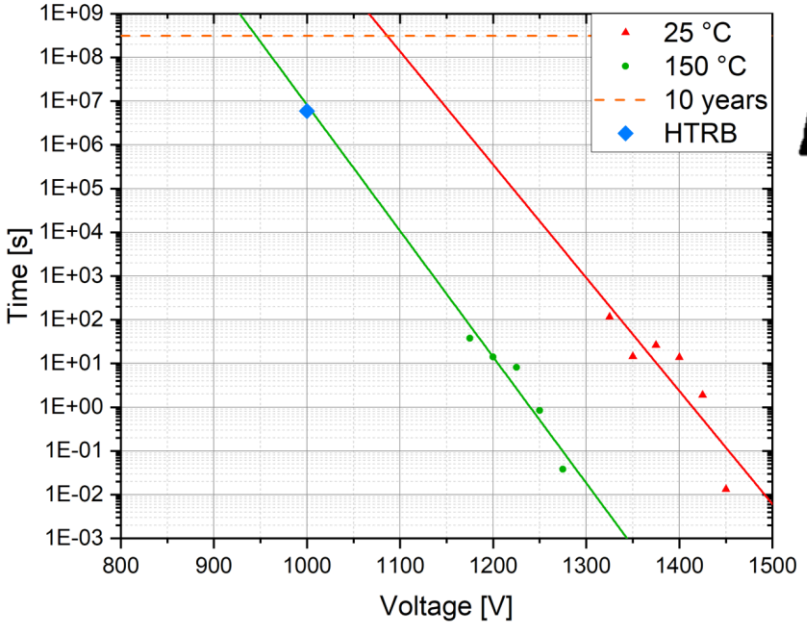
- Cost analysis (simple calculation)
  - Cost classic version: $€_{Classic} = k_{SiC} * A_{SiC0}$
  - Cost snubber version: $€_{Snubber} = k_{SiC} * A_{SiC1} + k_{Si} * A_{Si}$
  - Assuming chip size ratio $A_{SiC0}/ A_{Si} = 3/ 1$ (worst case taken from picture)
  - SiC chip size ratio directly linked to power losses ratio
    $A_{SiC0}/ A_{SiC1} = (P_{Classic,cond} + P_{Classic,switching})/ (P_{Snubber,cond} + P_{Snubber,switching})$
  - Assuming
    $A_{SiC0}/ A_{SiC1} = (50\% + 50\%)/ (50\% + ½ * 50\%)$
  - $€_{Snubber} < €_{Classic}$ (!)
  - → $k_{SiC} > 1{,}33 * k_{Si}$ (will be true forever!)
  - Plus additional savings on gate driver power

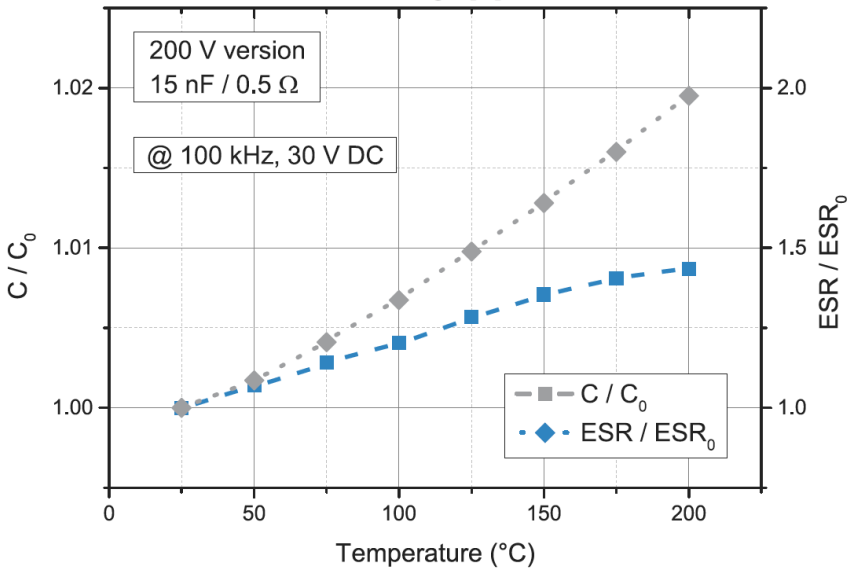
Technology Push: DC Link Cap for Integration

- Low energy density
- Low temperature coefficient
- Low isolation current
- High temperature capability
- Ready for integration



T. Becker, ECPE Online Workshop: Capacitors in Power Electronics, 2021



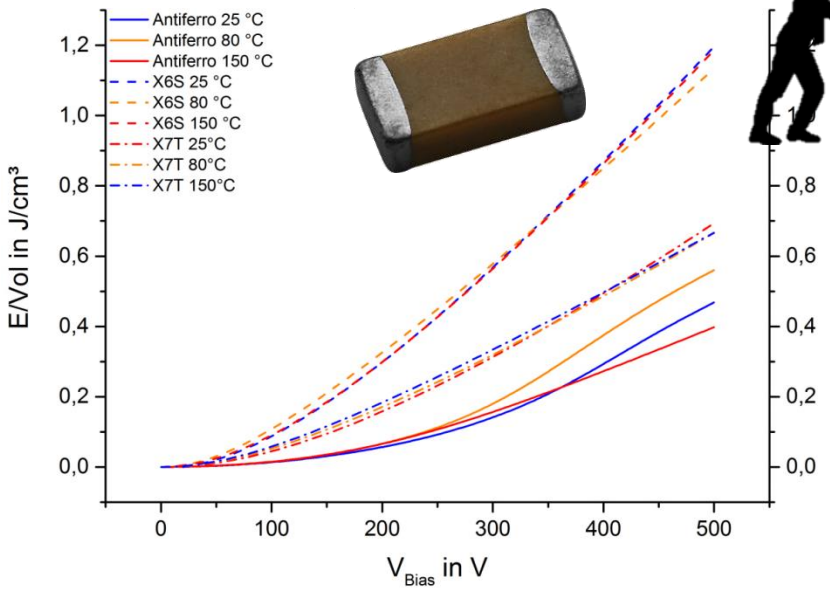


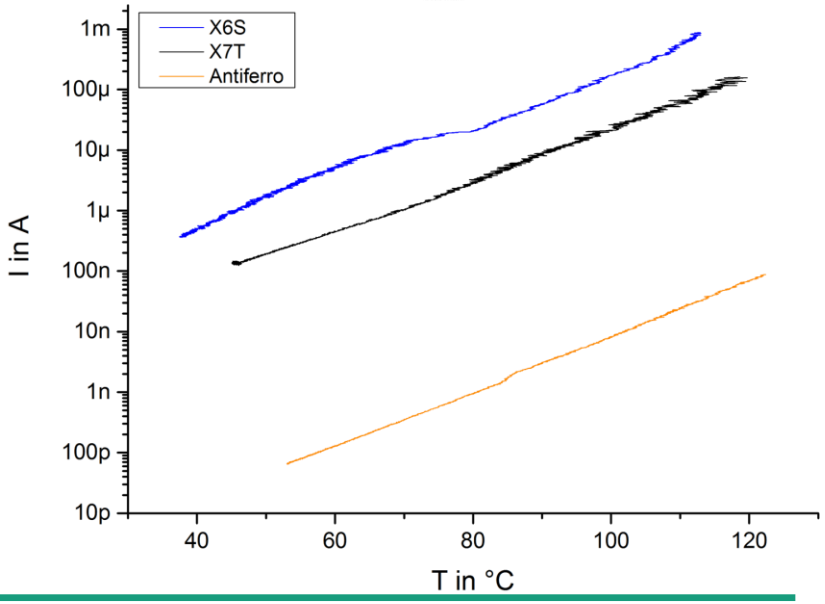
T. Erlbacher et al., WoDiM 2012, Dresden, GER

Fraunhofer IISB

Technology Push: Ceramic DC-link Capacitor

- Ceramic capacitors have outstanding energy density, low ESR, low ESL
- High nonlinearity capacitance over temperature and voltage depending on the material
- Calculated energy density is important (at a certain voltage level)
- Isolation current can be very high up to self destruction of the components (thermal runaway)
- Anti ferroelectric dielectrics (e.g. EPCOS CeraLink) seems to be as a good alternative for high temperature at moderate cost
- Temperature can go for > 200°C

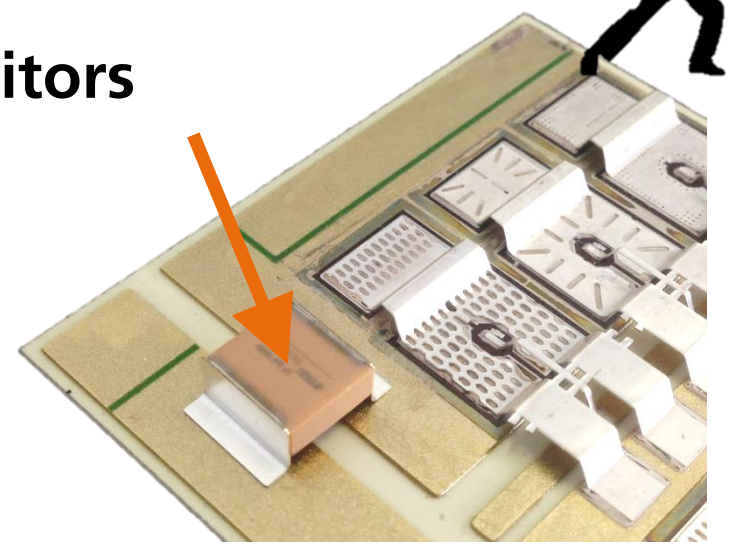




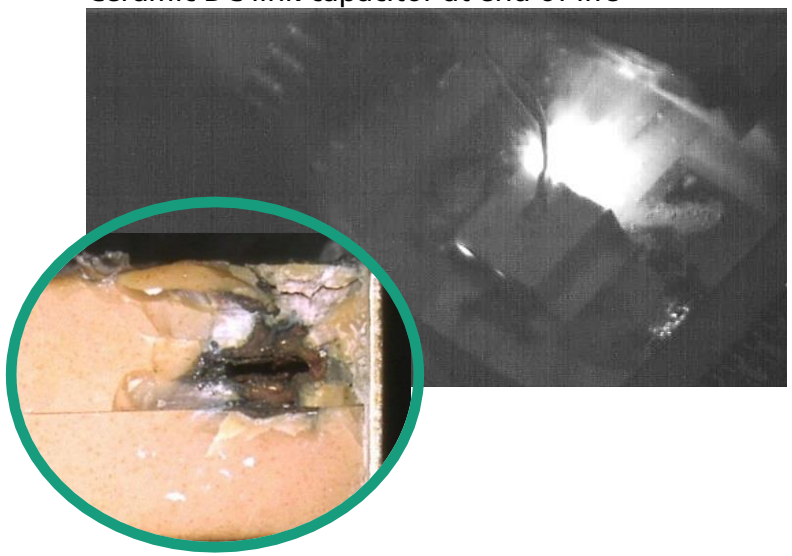
Fraunhofer IISB

Application Pull:
Active Power cycling tests - Capacitors

- Ceramic capacitors need soft termination because of mechanical stress (capacitor crack is a well known failure mechanism)
- Capacitors can have significant heating
  - passively by the power semiconductor → active PCT of active devices
  - active by own power losses → active PCT of passive devices



Ceramic DC link capacitor at end of life



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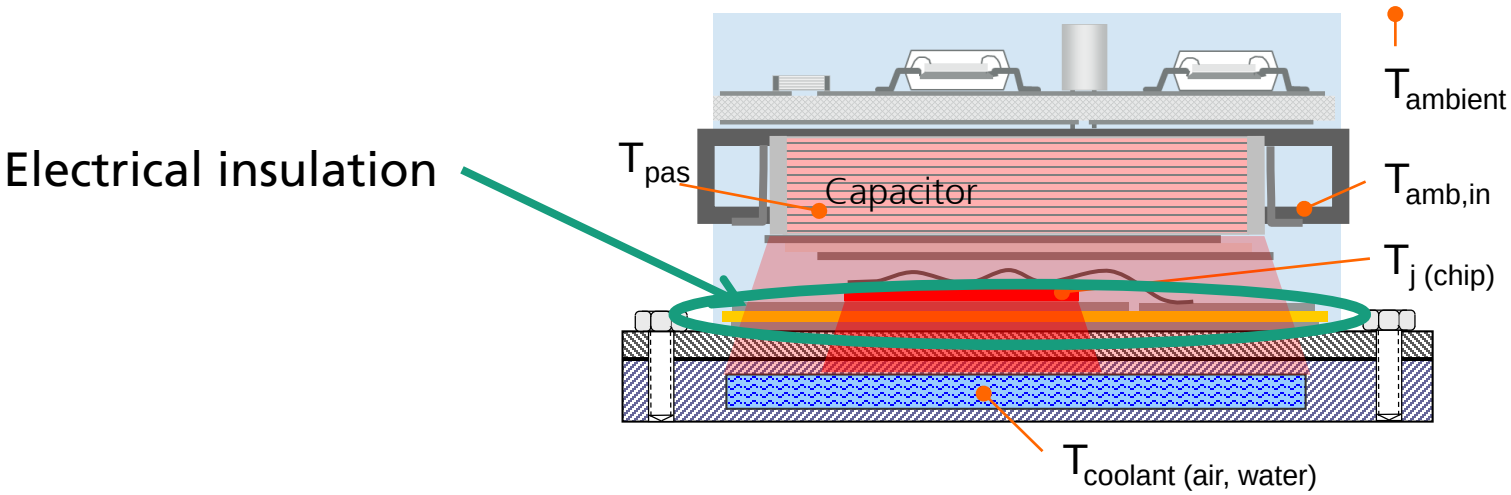
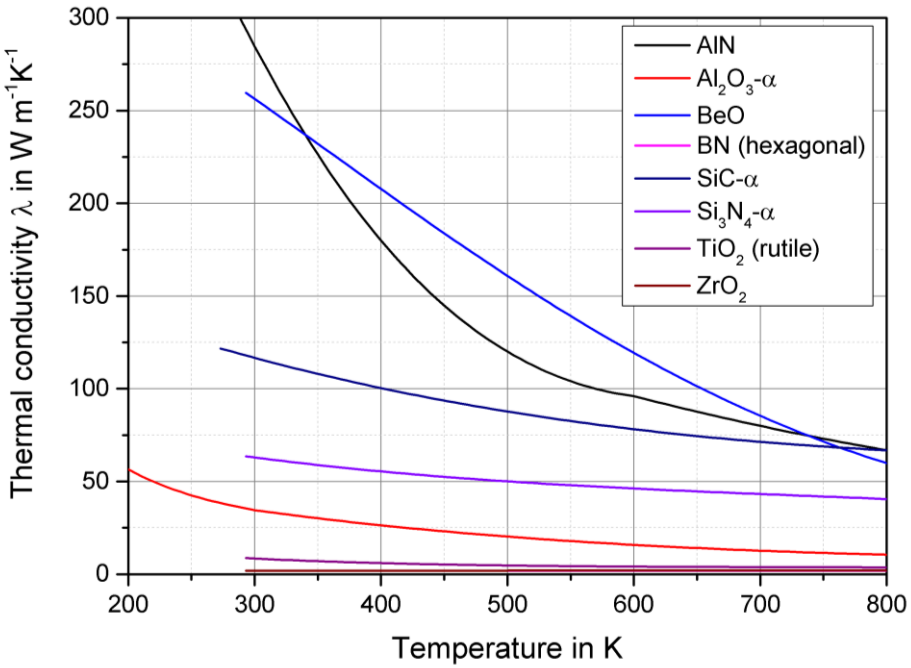
Integration: Electrical Insulation



Technology Push: Electrical insulation

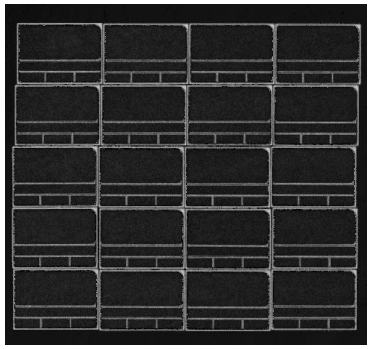
- Organic substrates
  - New PCB materials are available for temperatures up to 300 °C
- Inorganic substrates
  - Technologies like DCB, AMB, DAB on Al_2O_3, AlN, Si_3N_4
  - No temperature limit from the material
- Limitations in terms of temperature cycling (CTE mismatch)



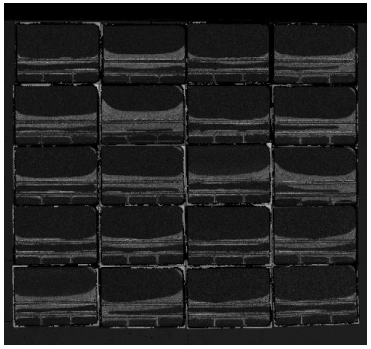
Technology Push: Electrical insulation

Passive Thermal Cycling Capability

- Al_2O_3 DBC @ -40/ 230 °C metallization delamination (concoidal fracture)

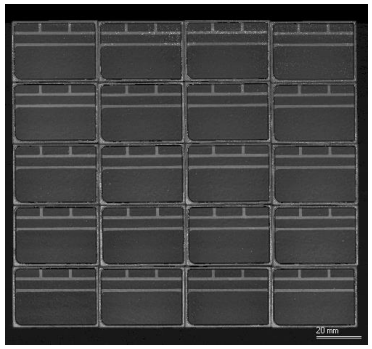


Initial state

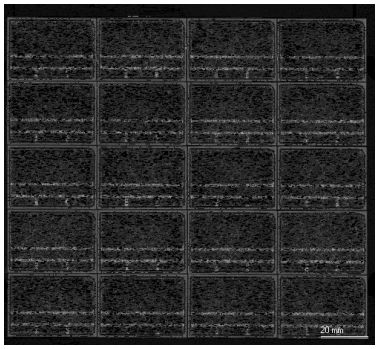


17 thermal cycles

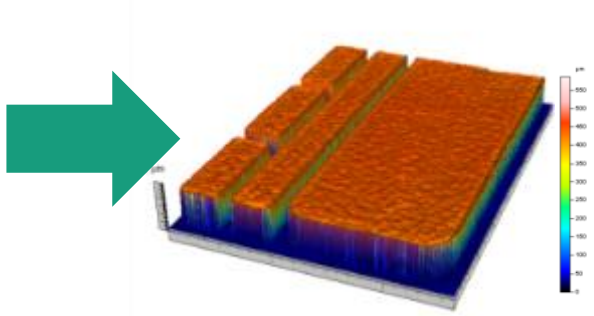
- AlN DBA @ -40/ 230 °C: no delamination



Initial state



983 thermal cycles

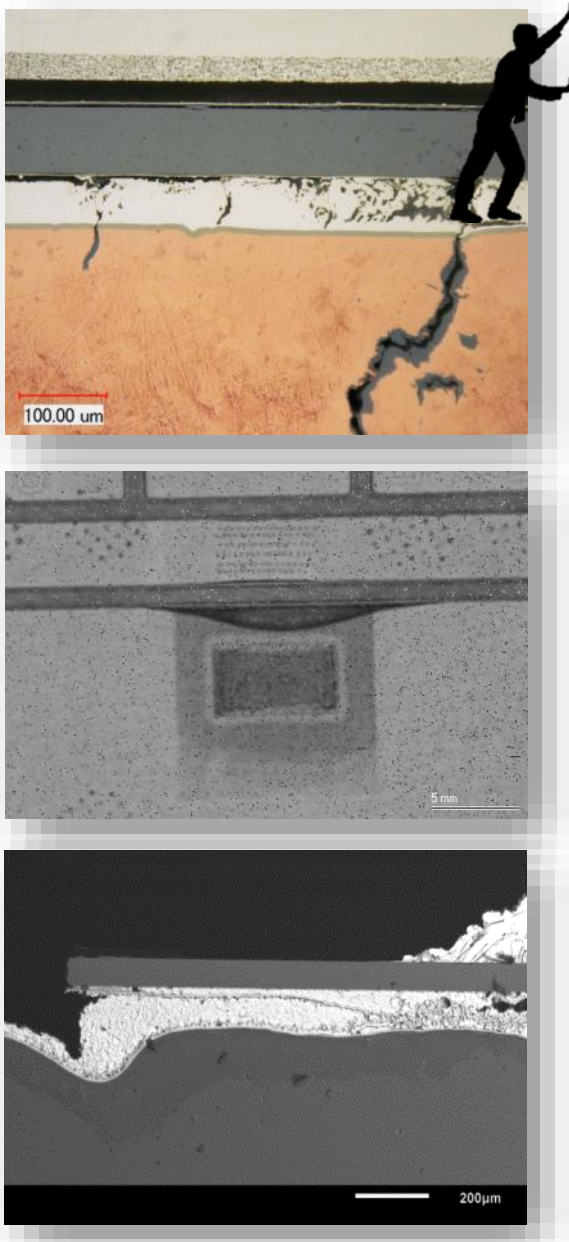


983 cycles → Rz ≈ 5.25 µm

Fraunhofer IISB

Technology Push: Electrical insulation (3)
Active Power Cycling Capability

- Impact on ceramic substrates
  - Failure mechanism for DCB, AMB
    - Vertical cracks in the substrate metal
    - Delamination of metal from ceramic
    - Concoidal fracture near the semiconductor die
    - Corrosion, oxidation, …
  - Failure mechanism for DAB
    - Recrystallization of the metal layer → Corrugated chip bond line

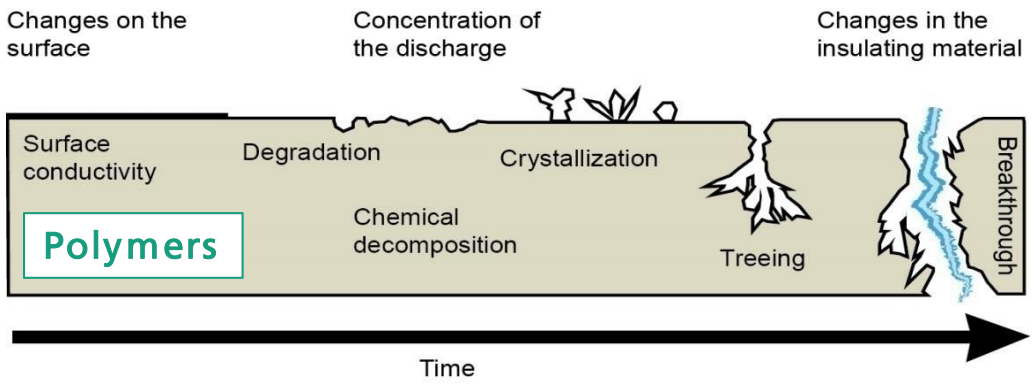


Picture source: Fraunhofer IISB
After Power Cycling Test with high dT and long lifetime: Top: DCB; middle DCB SAM; bottom DAB)

Fraunhofer IISB

Dielectric Breakdown in Insulation Materials

- From continuous partial discharge to material breakdown



- Breakdown mechanisms – intrinsic (µs), thermal (ms), erosion (h-a)
  - Dielectric strength in kV/mm (reference values)

Air	~3
Ceramics (AlN, Si_3N_4,Al_2O_3, etc.)	14 – 25
Potting (silicone gel, epoxy, etc.)	20 – 30
Transformer Oil	40 – 60

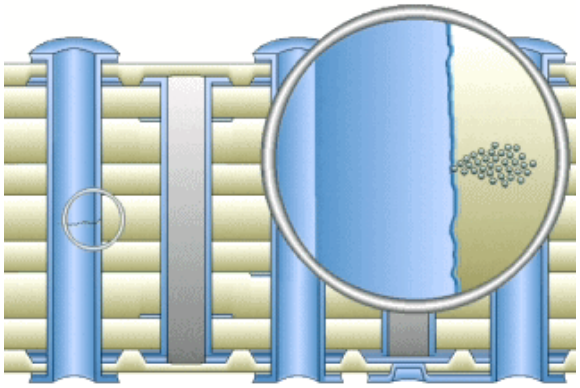
Corrosion on Insulating Substrates - Dentrides

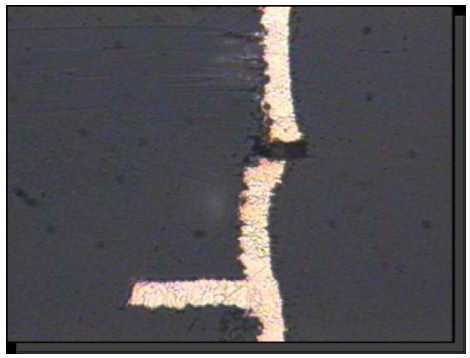
Fraunhofer IISB

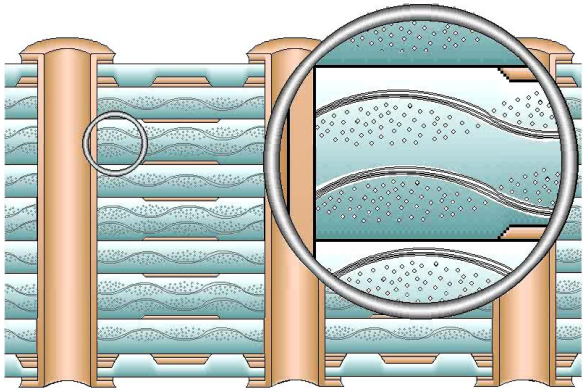
PCB Embedding – Failure Mechanisms

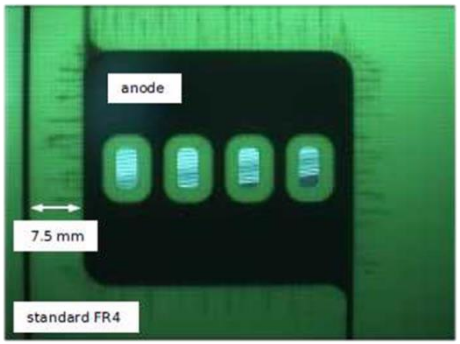
- Copper cracks in
  - Layers
  - all kind of vias
  - Vias/layer interconnections
- Delamination between
  - Embedded chips/ polymer
- CAF
  (Conductive anodic filament)
  - Vertical and lateral shorts
  - Groth of conductive filament along the glass fiber
  - Driven by temperature, humidity and electric fields
  - Driven by improper PCB manufacturing

All videos taken from http://www.pwbcorp.com/EN/portfolio.php









FR4 PCB after 730h CAF testing at 1500V, 85°C and 85% rH

Fraunhofer IISB

Technology Push: Joining Technologies, Die Attach (1)

- Alternative resins - bonding is extremely fast and polymers are available that can be processed from well under 200 °C to over 400 °C
- Electrically conductive adhesives - maximum operating temperatures between 200 °C and 350 °C but low electrical conductivity is less favorable
- Transient liquid phase diffusion bonding (Amalgam) - a bonding layer with a higher melting temperature than the bonding temperature, T_m of the interlayer and can be about 1000 °C (Ag_xIn_y, Au_xIn_y, Cu_xSn_y >350 °C)
- Welding, like wire-bonding (Al, Cu) tested up to 300°C
- Soldering - hundreds of materials and compound materials for soft soldering, as eutectic or non-eutectic solder materials ranging from 100 °C to 400 °C (melting temperature T_m)
- Sintering - high material limit of silver and already tested for temperatures up to 300 °C
- High lifetime, high temperature, big die size, chip to wafer die attach technologies for heterogeneous integration needed ;-)

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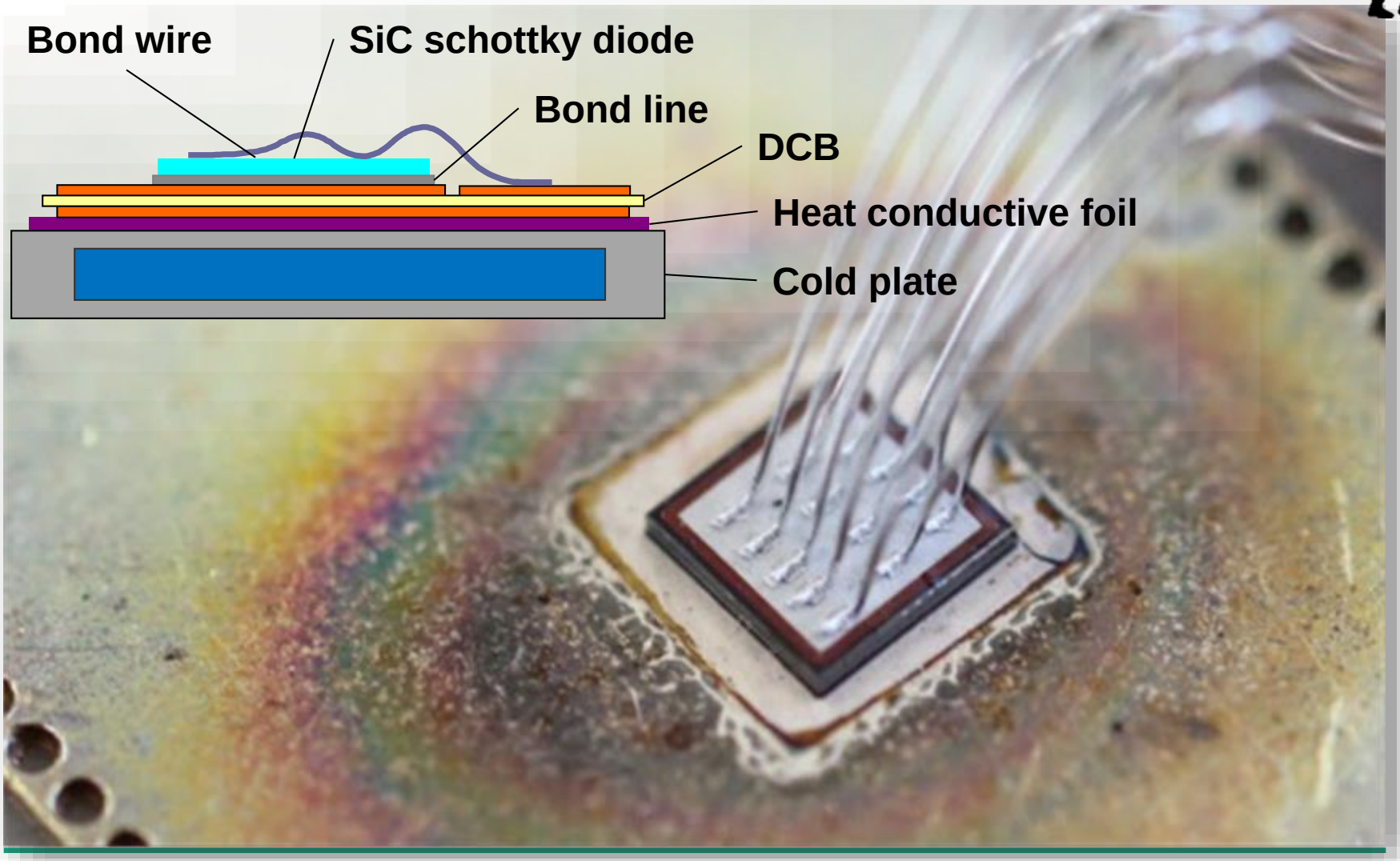
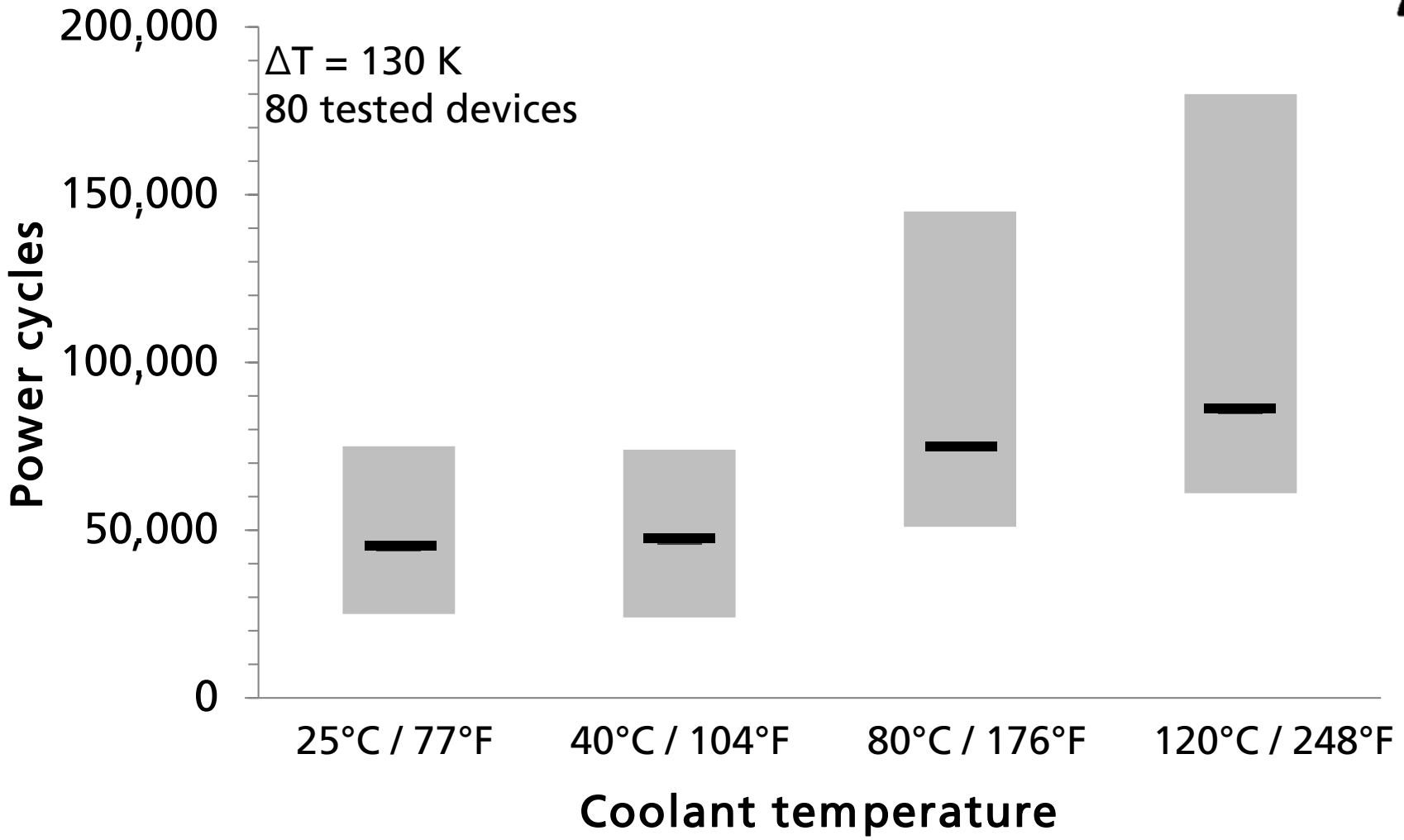
Die Attach Lifetime (1)



Die Attach, PCT Results: Silver sintering (4)



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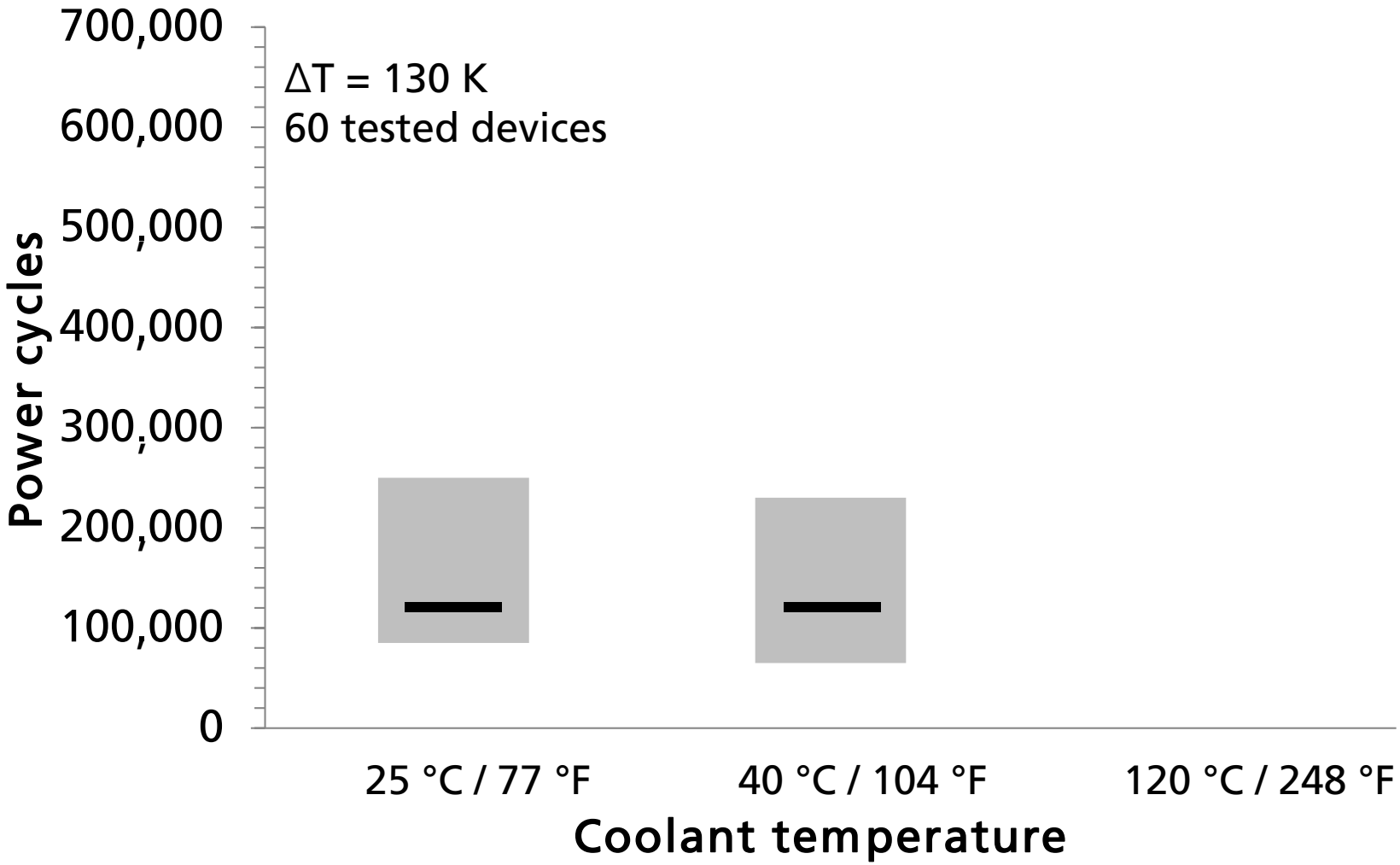
Die Attach, PCT Results: Gold-Germanium (5)

* No failure after 750,00 cycles



For comparison: Standard SnAgCu solder: 8,000 cycles at 40 °C / 104 °F

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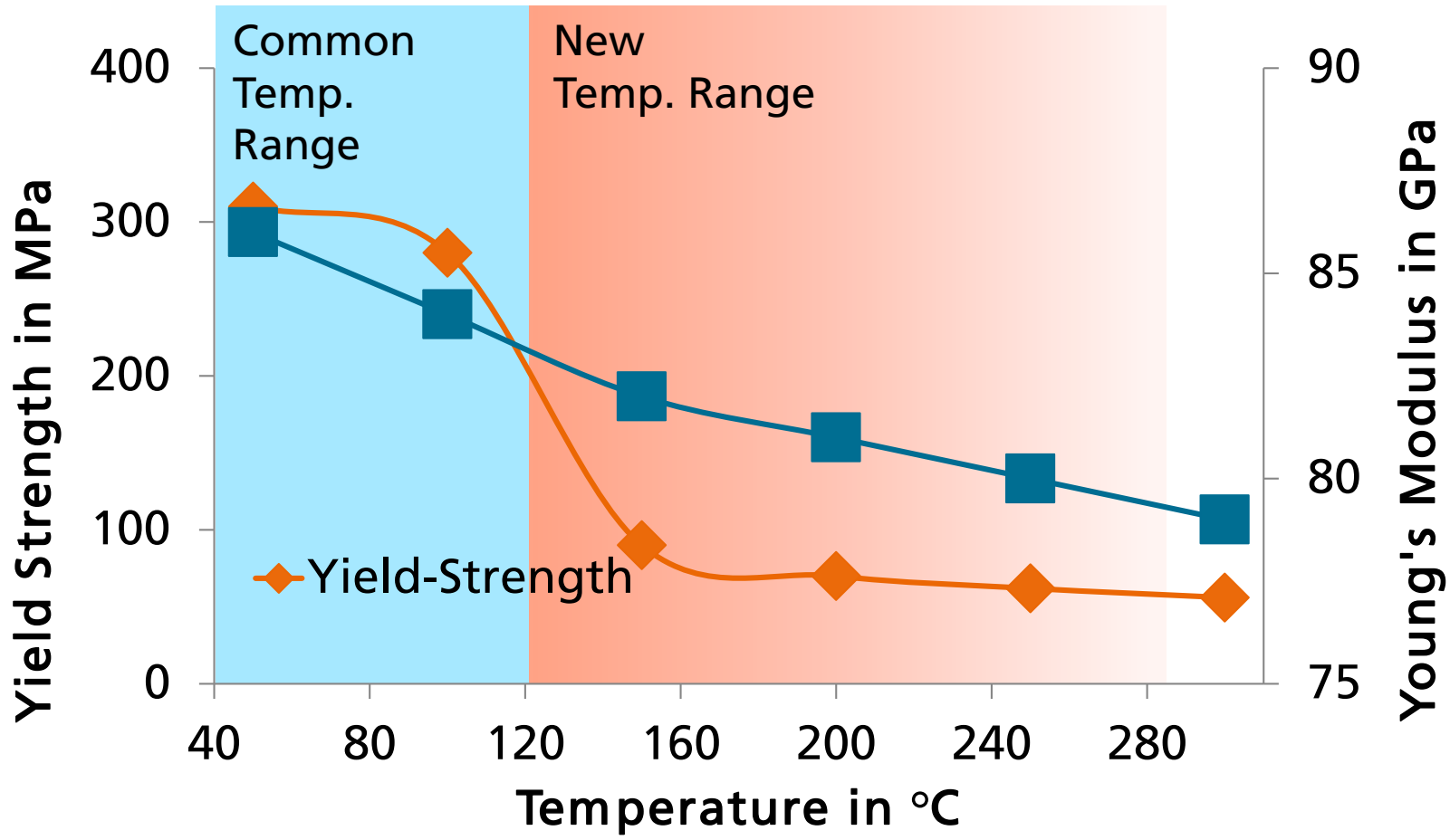
Die Attach, PCT Results Explanation (6)

Material Properties of Silver



Fraunhofer IISB

Conclusion

Take out advantage of high speed switching
Power electronics building block for easy use and cost reduction

Testability

Integration

Many materials in one package → lifetime

High electrical field strengths

Smaller footprint – same functionality

Smaller devices

High current density

High power losses density

High temperature

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