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FURTHER INVESTIGATIONS IN OPTICAL CONFINEMENT AND SOLAR CELL PROCESSING FOR CRYSTALLINE SILICON THIN FILM SOLAR CELLS

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ABSTRACT: This paper presents the investigations in the performance of different SiC and SiO_2 intermediate layer (IL) configurations during a zone melting recrystallisation (ZMR) step. The goal is to implement an IL consisting of an electrically conductive all-SiC multilayer stack in Recrystallised Wafer Equivalents (RexWE) solar cells. We tested stoichiometric SiC layers, carbon rich SiC layers and silicon rich SiC layers embedded in SiO_2 layers, temperature pre-treatments and several multilayer systems including all-SiC stacks. We also succeeded for the first time with a three layer SiC stack put together by PECVD to keep structural integrity throughout the ZMR process.
Further investigation on the potential of RexWE solar cells have also been made regarding the pitch in the laser fired rear access (LFA) process and the resulting series resistance as well as the increase in the short circuit current (J_{sc}) due to a plasma texture.

Keywords: Optical confinement, Intermediate layers, c-Si Thin Films, SiC

1 INTRODUCTION

For crystalline silicon thin-films in applications such as our Recrystallised Wafer Equivalent (RexWE) [1], excellent optical confinement is essential. As the photoelectrically active bulk in this concept is usually only 10 – 20 µm thick, light with wavelengths exceeding 600 nm already exceeds this film thickness.
Along with front side texturisation, the rear side needs to be highly reflective for long wavelength light. The effect of light trapping on the percentage of absorbed photons as well as the potential gain in short circuit current (J_{sc}) is shown in [2] for a related crystalline silicon thin-film concept.
In the RexWE the active silicon bulk layer is formed on top of a possibly contaminated substrate, so the rear side of the bulk has to be terminated by an intermediate layer (IL). This IL needs to act as a diffusion barrier with sufficiently high electrical conductivity, as an excellent optical reflector, and ideally also as a passivation layer for interface defects.
For sophisticated light trapping purposes we study functional multilayer stacks deposited by plasma enhanced chemical vapour deposition (PECVD). Several layers of either SiC or SiO_2 with distinct optical properties such as refractive index and film thickness can be deposited and studied for this purpose as shown in Fig. 1. These stacks are tailored with layers having alternating high/low refractive indices. The specially designed reflection properties can be realised by controlling the various layer stoichiometries, and thus refractive indices, as well as the number and thicknesses of the layers in the stack.
In order to fabricate RexWE solar cells the IL layer stacks are subjected to a process sequence including Si seeding layer deposition, zone melting recrystallisation (ZMR) [3] and epitaxial Si growth. During these processes the samples and thus the IL are heated and thereby have to withstand temperatures up to the melting point of silicon (1400 °C) while having to preserve the structural integrity of the constituent layers.
We previously showed that all-SiC reflectors consisting of various SiC-layer stacks were not stable enough to withstand the ZMR process [4,5]. However a reflector stack, consisting of a high refractive index silicon rich SiC layer embedded between two low refractive index SiO_2 layers performed very well during the ZMR process. The crystallisation and furthermore the solar cell processing produced the results presented in [5], including efficiencies of up to 11.1 %. For stacks including SiO_2 the lack of electrical conductivity is bypassed by drilling holes through the stacks and the already recrystallised layer using a laser as depicted in Fig. 1 (right). We call this process laser-fired rear access (LFA).

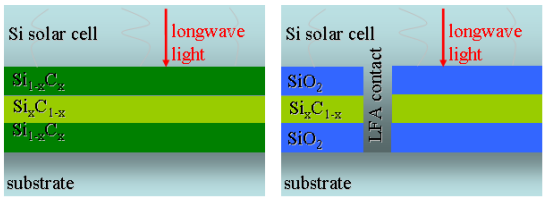

Figure 1: Left: Schematic of all-SiC electrically conductive multilayer stack. Right: SiO_2/SiC/SiO_2 stack with laser fired rear access contact formation.

The laser process is an obvious disadvantage of the reflectors including SiO_2 which not only raises processing costs but also compromises the diffusion barrier properties. Comparatively the layers in all-SiC stacks can be doped and thus made electrically conductive [6]. Therefore all-SiC multilayer stacks are the explicit motivation for the investigations in this paper.

2 INTERMEDIATE LAYER EXPERIMENTS

2.1 Layout of experiment

For the following results the substrate chosen was highly p-doped ($4 \cdot 10^{18}$ cm^{-3}), multicrystalline Si wafers of 100 x 100 mm^2. The deposition of the multilayer reflectors was done with PECVD. The plasma reactor used for SiC deposition operates with a combined radio-frequency (13.56 MHz) and a microwave (2.45 GHz) source using precursor gases CH_4 (methane) and SiH_4 (silane). The reactor for SiO_2 deposition has a parallel

plate (rf) setup.
After the deposition of the various ILs on the 10 x 10 cm^2 samples, a highly doped Si seeding layer was grown from the gas phase (RTCVD) and subsequently capped with a 2 µm thick SiO_2 layer, also grown by PECVD. The fine grained seeding layer was then recrystallised by ZMR and characterised.

2.2 Reflector development

A set of samples including the IL configurations shown in Fig. 2 was prepared. As the aim is to implement an all-SiC multilayer stack in a RexWE solar cells this configuration was the starting point of the experiments. The all-SiC stack consisted of a carbon rich SiC layer (115 nm), a silicon rich SiC layer (150 nm) and another carbon rich SiC layer (140 nm) as shown in Fig. 2 (middle).

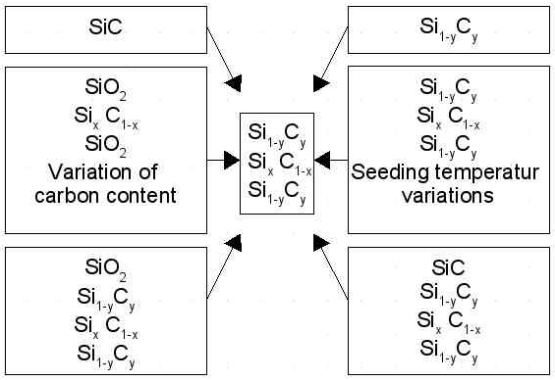

Figure 2: SiC intermediate layer configurations used for stability test during zone melting recrystallisation, aiming towards the utilisation of the all-SiC multilayer stack in the middle. For the ZMR step each of the shown intermediate layer configuration is sandwiched between the seeding layer on top and the substrate beneath.

The single layer of stoichiometric SiC (300 nm) (Fig. 2 upper left) was chosen as a reference, as it has previously been proven to be stable and reliable. Also the SiO_2 (150 nm) - silicon rich SiC (120 to 140 nm) - SiO_2 (150 nm) stack (Fig. 2 middle left) has been proven to be applicable in a RexWE solar cell. In this experiment we investigated the dependence of the carbon content of the SiC layer on the high temperature behaviour. In order to separate the roles of each layer in the detrimental effect of the all-SiC stack a single carbon rich SiC (115 nm) layer (Fig. 2 top right) has also been tested. The all-SiC stack has also been tested in conjunction with different temperature loads during the seeding layer deposition in order to pre-temper the SiC layers (Fig. 2 middle right).

Additionally all-SiC stacks have been topped with either a reference stoichiometric SiC layer (300 nm) (Fig. 2 lower right) or an SiO_2 layer (250 nm) (Fig. 2 lower left). Both top layers have already proven to withstand the ZMR process as single layers.

2.3 Recystallisation

As stated in previous papers [4,5] all-SiC IL stacks showed blistering effects which led to holes in the recrystallised layer. This blistering was first thought to be dependent on the hydrogen content of the layers, so several tests using higher power densities of the rf-source during the deposition process have been conducted. Nevertheless no successful recrystallisation process could be established even with the denser layers incorporating less hydrogen.
To get more insight into the blistering phenomena Fig. 3 shows a cross section SEM picture of a sample after an unsuccessful ZMR process. The picture shows the region of the sample where the seeding layer, approximately 10 µm thick, on top of an IL should be located. Instead, no IL but thin white lines throughout this whole region can be observed. An EDX scan across one of those white lines showed a silicon carbon mixture for a length of approximately 400 nm within a silicon bulk.

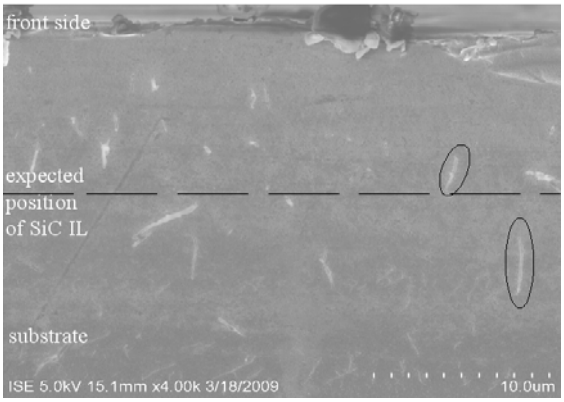

Figure 3: Cross section SEM picture of sample in which IL lost structural integrity during the ZMR step. Two SiC IL fragments marked with black circles.

As the higher carbon content as well as the measured thickness is consistent with the expectations for the IL it can be concluded that the white lines are the remaining fragments of the IL. Due to their spreading throughout the whole seeding layer thickness, a total integrity failure of the IL and a subsequent dispersion in the liquid silicon phase can be assumed.

2.4 Temperature pre-treatment

A temperature treatment right before a ZMR step was found to be beneficial. It was observed that after exposure to a temperature only a few degrees below the melting point of the seeding layer, a subsequent ZMR step could be conducted successfully. However, to achieve reproducibly is difficult because the temperature range for the pre ZMR temperature treatment seems to be very narrow. If the temperature is too low then it has no positive effect on the subsequent ZMR step and if the temperature is too high then the silicon melts just like in the ZMR step itself which results of course in the known blistering effect. So far no process has been found that is accurate or homogeneous enough in temperature to pre-treat areas large enough for further solar cell processing.
Nevertheless Fig. 4 shows a SEM picture of a cross section with a three layer all-SiC stack after successful recrystallisation. The IL displays the expected continous coverage of the substrate surface. With higher magnification (see inset in Fig. 4), one can clearly distinguish the three single layers showing a crystalline structure. One hypothesis for the benefit of a temperature pre-treatment is that at temperatures close to the melting point of the silicon seeding layer the ILs, grown by PECVD, start to crystallise and become therefore much more temperature stable.

Encouraged by this result we prepared a set of samples including all-SiC multilayer stack ILs on which we varied the temperature during the seeding layer deposition. The deposition temperature ranged from standard 920 °C up to a maximum possible 1100 °C. This temperature load was apparently not sufficient because during the ZMR the same blistering phenomena were still observed.

2.5 Silicon and carbon rich SiC

To investigate the failure of the all-SiC stack, several configurations all consisting of top and bottom SiO_2 layers that encapsulate SiC layers with varable silicon content were tested. All these layers (partly already shown in [5]) allowed more or less stable recrystallisation processes. A further result from these tests was that with increasing silicon fraction in the silicon rich SiC layer, the ZMR process turned out to be more stable. As the silicon rich SiC layers seemed to be stable during the ZMR process we investigated further the behaviour of the carbon rich SiC layers. For this purpose carbon rich SiC-layers were deposited as single ILs and then subsequently recrystallised. This simple configuration did also not withstand the ZMR process and showed severe occurrence of blistering i.e. IL integrity failure.

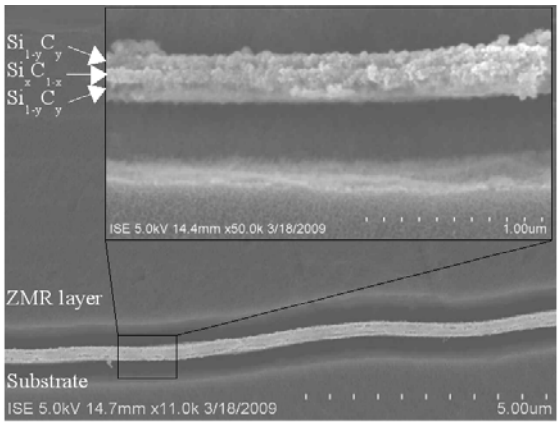

Figure 4: Cross section of three layer all-SiC stack after successful ZMR process.

2.6 Stoichiometric SiC

In contrast to these results for silicon and carbon rich layers it has been shown previously and was evident again in this work, that a single layer of PECVD stoichiometric SiC functions very well as an IL in a RexWE. It only lacks the high end reflection properties. Samples with single layers of stoichiometric SiC for an IL have in course of these experiments successfully been prepared with the standard ZMR process serving as another reference process. This stoichiometric SiC layer proved to be reliably incorporated in a ZMR process.

To elicit further possibilities for multilayer stacks the three layer all-SiC stack has been topped with a layer of either stoichiometric SiC or an SiO_x layer. The stoichiometric SiC used for the top layer was the same as that referred to in successfully recrystallising with the single layer of stoichiometric SiC. However in this multilayer stack configuration, the stoichiometric SiC was not able to conserve the integrity of the whole SiC stack. Again there was massive blistering visible in the liquid silicon phase during the ZMR process. This was probably due to the temperature load for the carbon rich SiC underneath which was still too high.

2.6 SiO_2 top layer on all-SiC stack

In contrast, the configuration where a three layer all-SiC stack was topped with an SiO_2 layer showed very good results in terms of IL and recrystallisation process stability. The first hypothesis that comes to mind is that as a top layer the SiO_2 reflects more light than the SiC so that the carbon rich layer underneath can keep its integrity. This was the first time a multilayer SiC stack deposited by PECVD maintained its integrity on a large scale throughout a ZMR process. With this result and matrix field simulations a new set of IL can be designed to further increase the back side reflection of our RexWE.

3 SOLAR CELL PROCESSING AND RESULTS

So far only samples with silicon rich SiC layers embedded between two SiO_2 layers have been processed to solar cells. To establish electrical conductivity through the IL incorporating SiO_2, holes were drilled through the already recrystallised seed layer and the IL using a laser. This way the later solar cells can be contacted with the classic front side grid and a full metallised back contact scheme. After lasering, the samples were stripped of the capping oxide and the seeding layer was partially etched back with a CP 33 etch (HNO_3, 70 % / CH_3COOH, 100 % / HF, 50 %). The solar cell base was then grown epitaxially on all samples with a designated thickness of 15 µm and a doping concentration of $8 \cdot 10^{16}$ cm^{-3}. The samples were subsequently cut to 25 x 25 mm^2 to undergo the further solar cell processing.

The solar cell process starts with plasma texturing in a large area plasma reactor using an established process that consumes only 2 µm of Si [7]. The samples were then diffused in a tube furnace at 830°C using $POCl_3$ gas creating an 80 Ω/sq. emitter. This emitter was passivated with a thin thermal oxide which was opened using photolithography to evaporate the Ti/Pd/Ag contact fingers. The rear-side of the RexWE was evaporated with 2 µm of aluminium. After electroplating and sintering at 400 °C the samples were cut to 20 x 20 mm^2 to achieve edge isolation and the bulk was subsequently passivated with remote plasma hydrogen passivation (RPHP) at 390°C [8]. To further enhance the optical confinement a double layer anti-reflection coating (DARC) (MgF/TiO_x) was evaporated on all solar cells.

The process step of etching back the seeding layer thickness was introduced because a back reflector is more beneficial the thinner the seeding layers are. However a thicker seeding layer is deposited with better homogeneity and therefore the ZMR step is more stable. All samples were therefore deposited with approximately 7-8 µm silicon, recrystallised and subsequently etched back. In characterising tests the CP 33 etch revealed an etch rate of 4 µm/min. The recrystallised layers showed due to the seeding deposition process very inhomogeneous layer thicknesses where at even after 45 seconds (estimated 3 µm etch back) parts of the seeding layers were already removed while other parts were still some µm thick. This led to a loss of much of the sample area which was up to that point well prepared. This also constrained further process variations and

statistics. In future experiments a more reliable seeding deposition and ZMR process on thin seeding layers will be chosen over an etch back process.

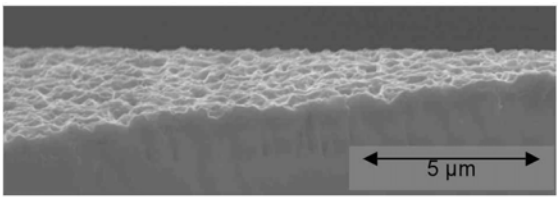

Figure 5: Cross section SEM picture of plasma textured surface on RexWE solar cell.

To further investigate the potential of the given RexWE set up we evaluated the effects due to the variation of the laser hole pitch. The bulk grown on top of the lasered via holes is probably significantly lower in quality, therefore the amount of holes should be as small as possible, i.e. the hole pitch should be maximised. On the other hand, the conductivity of the bulk and seeding layers set an upper limit to the hole pitch. To find an optimum two sets of samples were fabricated, one with a hole pitch of 3 mm in a honeycomb like pattern, the other in the same manner with only 1.5 mm pitch. The measurements of the finished solar cell properties were evaluated by fitting a two diode model to the dark I-V curve. The so calculated series resistance (R_s) showed an average over all samples (regardless of the laser hole pitch) of 0.23 Ωcm^2 with a standard deviation of 0.06 Ωcm^2. With the given current values of up to 23.8 mA/cm², no difference in the R_s whether a 3 or a 1.5 mm pitch was applied could be seen. A beneficial effect due to a smaller area fraction affected by the laser drilling in the 3 mm pitch case was also not observed. This is due to other more dominant process inhomogeneities affecting the open circuit voltage (V_{oc}), short circuit current (J_{sc}) and fill factor (*FF*).
In the course of this experiment we evaluated the benefits due to a plasma texturing of the front surface. From a total number of fourteen samples half were textured as described in [7] with SF_6, O_2, NH_3. A SEM picture of a textured surface can be seen in Fig 5. This texture shows a very small feature size but it is still able to significantly lower the total reflection while also raising the fraction of diffuse reflection to almost 100 % of the total reflected light. The percentage of diffuse reflection is also an indicator that the light coupled into the silicon is deflected from the shortest path through the bulk, hence improving the light trapping. Even after the deposition of the DARC where the reflection is lowered to 2.5 % at 700 nm on all samples, an average benefit in J_{sc} for the textured samples of 1.4 mA/cm² with a standard deviation of 0.8 mA/cm² was seen. The untextured samples showed thereby a mean J_{sc} of 21.2 mA/cm² with a standard deviation of 0.8 mA/cm².

Tab. 1: Best RexWE solar cells (20 x 20 mm^2) with a diffused emitter (80 Ω/sq.), plasma texture and a DARC.

Reflector	**V_{OC} [mV]**	**J_{SC} [mA]**	**FF [%]**	**η [%]**
SiO_2/SiC/SiO_2	559	23.8	72	9.5

Due to unrelated processing problems, overall cell efficiencies, V_{oc}, J_{sc} *and FF* were lower than previously reported. The solar cell properties of the best cell are shown in Tab. 1.

4 CONCLUSIONS

We investigated the performance of different SiC and SiO_2 intermediate layer (IL) configurations during a zone melting recrystallisation (ZMR) step. With regard to the goal of an IL consisting of an all-SiC multilayer stack we found that even single carbon rich layers are not per se able to withstand temperatures exceeding 1400 °C. A pre temperature treatment before a ZMR step probably leads to crystallisation and thereby strengthening an all-SiC stack thus allowing successful recrystallisation. But as this pre ZMR temperature treatment is very temperature sensitive only small areas could be successfully processed so far. For the first time a three layer SiC stack put together by PECVD, kept its structural integrity throughout a ZMR process.
Also for the first time even on larger scales a three layer all-SiC stack, although topped with an SiO_2 layer was successfully recrystallised. Therefore new simulations can be carried out to further optimise the reflection properties of the IL.
Additionally further investigations on the potential of Recrystallised Wafer Equivalents solar cells have been made. Thereby the series resistance of a RexWE with laser fired rear access is not limited when expanding the laser pitch from 1.5 to 3 mm in a honeycomb pattern. And even after the deposition of a double layer anti reflection coating a plasma texture raises the short circuit current by an average of 1.4 mA/cm².

5 ACKNOWLEDGEMENTS

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6 REFERENCES

[1] S. Janz, S. Reber, H. Habenicht, H. Lautenschlager, C. Schetter, „Processing of c-Si Thin-Film Solar Cell on Ceramic Substrate with Conductive SiC Diffusion Barrier Layer“, *4th WCPEC*, Hawaii (2006), pp.1403-1406.

[2] F. Duerinckx, H. Van Nieuwenhuysen, H. Kim, I. Kuzma-Filipek, H. Dekkers, G. Beaucarne, J. Poortmans, “Large-area Epitaxial Silicon Solar Cells Based on Industrial Screen-printing Processes” Prog. Photovolt: Res. Appl. 2005; 13:673–690.

[3] T. Kieliba, „Zone Melting Recrystallization for CSiTF solar cells“, *Verlag im Internet*, Berlin (2006), ISBN 3-86624-196-8.

[4] S. Janz et al., "Optical Confinement in Crystalline Silicon Thin-Film Solar Cells", *22nd EU-PVSEC*, 2007, pp. 1979-1982.

[5] S. Janz , M. Kuenle , S. Lindekugel , E. J. Mitchell, "Advanced Optical Confinement and Further Improvements for Crystalline Silicon Thin Film Solar Cells", *33rd IEEE-PVSEC*, 2008, pp. 168- 172.

[6] S. Janz, "Amorphous Silicon Carbide for Photovoltaic Applications", *Verlag Dr. Hut*, München (2007), ISBN 978-3-89963-563-8.

[7] S. Lindekugel, E. Schmich, S. Janz, S. Reber, "Plasma Texturing of Low Defect Epitaxial Layers", *22nd EU-PVSEC*, 2007, pp. 1986-1989.

[8] S. Lindekugel, H. Lautenschlager, T. Ruof, S. Reber, "Plasma Hydrogen Passivation for Crystalline Silicon Thin-Films", *23nd EU-PVSEC*, 2008, pp. 2232-2235.