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SURFACE PASSIVATION OF SILICON SOLAR CELLS USING AMORPHOUS SILICON CARBIDE LAYERS

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ABSTRACT

Dielectric layers for the passivation of solar cell surfaces are a crucial component of future cell generations. Not only their electrical and optical properties are of importance but also the implementation into an industrial cell process. In this regard an easy preconditioning of the surface, low process temperature and high thermal stability are essential. Therefore, we have developed a new passivation process based on PECVD deposited SiC_x. The cleaning of the surface was performed in-situ in the plasma chamber. Excellent passivation quality ($S < 5$ cm/s) was achieved even though no additional wet chemistry cleaning was applied. Although the deposition temperature is in the range of 300-400°C, high thermal stability could be demonstrated. A solar cell structure with SiC_x as rear surface passivation exhibited an implied open-circuit voltage of 679 mV after a firing step of 800°C. Cells using a single SiC_x layer and laser-fired contacts as rear surface structure have shown very high efficiencies of 20.2%.

INTRODUCTION

In order to reduce the cost of photovoltaic energy conversion from mono- and multicrystalline silicon solar cells, efficiencies have to be increased and wafer thickness has to be decreased. A crucial component of the cell for the realization of such goals is the rear surface due to the increasing demands for optical (internal reflection) and electrical quality (surface passivation). The standard structure for state-of-the-art industrial cells is an aluminum back surface field (Al-BSF) created by firing a screen-printed Al paste. Although this process is well suited in terms of industrial feasibility, it can not be used for future generation cells with efficiency levels above 18% and wafer thicknesses below 150 µm. This is due to the relatively poor electrical and optical properties [1] which will limit the cell performance on thin substrates. Additionally, the wafer bow caused by the Al firing process is a severe problem. Thus, it is quite obvious that future generations of industrial cells will use the same rear surface structure as the one introduced for high-efficiency lab cells a couple of decades ago: the dielectric surface passivation. As the related local contact formation is industrially feasible using the laser-fired contact (LFC) process [2], one question is still open: "What is the optimal dielectric passivation layer?". This question has to be answered not only in terms of electrical and optical quality of the different layer systems, but also in respect of application in cell structures and processes. If a dielectric rear surface passivation has to be combined with a standard screen-printed front surface metallization, a critical factor is the stage in the process sequence where the layer will be deposited (see Fig. 1).

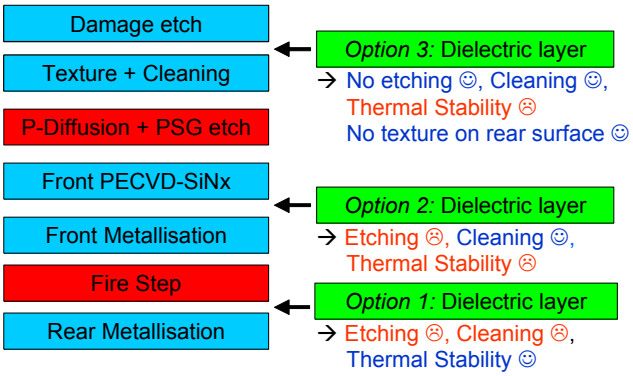

Fig. 1. Formation of a dielectric layer within an industrial solar cell process.

INTRODUCING THE FABRICATION OF A DIELECTRIC LAYER WITHIN A SCREEN-PRINTING PROCESS

Depositing the dielectric layer on the rear surface after the firing step for the front metallization (option 1 in Fig.1) requires a strong surface conditioning, including etching of the rear emitter layer and severe cleaning since the wafer has already been subject to several "dirty" process steps at that stage. Thus, although the dielectric layer will not see any high-temperature step afterwards, it is a difficult task to obtain good surface passivation.

Alternatively, the layer could be deposited after the emitter diffusion (option 2 in Fig.1) as a sort of natural choice since the front surface nitride deposition is performed at the same stage. Although the wafer is in clean conditions, the rear emitter layer has to be etched away and the layer has to withstand a high-temperature step i.e. the firing step.

An even more elegant option could be the layer deposition before the emitter diffusion (option 3 in Fig .1). At that point the wafer is definitely clean and no emitter layer has to be etched away. Additionally, the passivation layer will mask diffusion and if the etching sequence is chosen in a clever way, also texturization on the rear surface will be avoided. It was shown that the passivation quality on a non-textured surface is significantly better [3,4]. Thus, this process sequence seems to be ideal but of course the passivation layer has to withstand two high-temperature steps without losing its passivation quality.

Therefore besides good electrical and optical properties, a high thermal stability is essential for an industrially feasible passivation layer.

DIFFERENT DIELECTRIC LAYERS

The classical choice for a passivation layer with good thermal stability is a silicon dioxide layer thermally grown at temperatures between 800°C and 1050°C: This layer was used for our first test to transfer the LFC technology into an industrial process sequence [5]. However, due to the high process temperature it could be difficult to use this process in an industrial environment although it was shown that an oxidation at reduced temperatures does not degrade material quality [6] and that in-diffusion of surface contaminants is less critical than thought before [7].

A process closer to today's industrial reality is the deposition of silicon nitride using PECVD. However, it was not possible to reach the same passivation quality as for thermal oxides when applied to a solar cell due to detrimental shunting of the inversion layer induced by the SiN_x-layer [8]. Also thermal stability seems to be an issue although recent works have shown that a medium passivation level can be kept after a firing step [9].

SiC_x is well-known to be quite stable with respect to thermal treatments. In fact it is used at Fraunhofer ISE as a diffusion barrier layer for recrystallization of silicon thin-film layers on low-cost substrates [10]. Recently, Martín *et al*. [11] reported that SiC_x also shows good passivation quality (S < 30 cm/s). After a firing step at 730°C, the passivation quality was not decreased. Thus, this material type could be extremely interesting but it has to be shown that it works effectively not only on lifetime samples but also in solar cells.

SIC_X LAYERS OPTIMIZED FOR INDUSTRIAL APPLICATION

Passivation Quality and In-situ Cleaning

The PECVD system used for SiC_x deposition at Fraunhofer ISE offers the possibility to perform an in-situ plasma cleaning step prior to the deposition itself. 1 Ω cm p-type high-lifetime FZ-Si wafers were used to optimize this process. The wafers were taken out of the box and plasma-cleaned. Subsequently, the SiC_x-layer was deposited without any additional wet-chemical process. The passivated wafers were characterized using the QSSPC [12] and the CDI/ILM method [13, 14]. In Fig. 2 a lifetime histogram extracted from a CDI/ILM lifetime map is shown. Not only very high average lifetimes were achieved but also a very narrow distribution which shows that the plasma cleaning is very efficient and homogeneous [15].

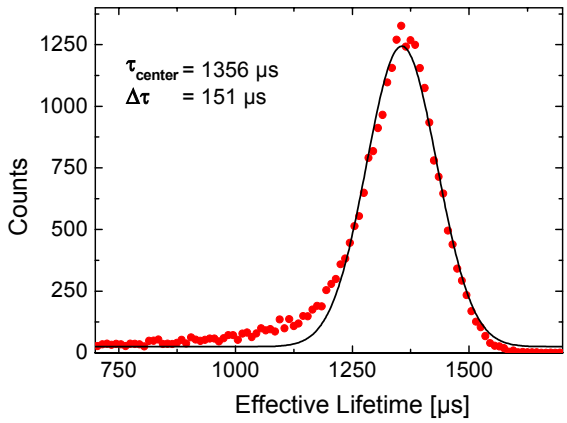

Fig. 2. Spatial lifetime distribution on a 4" 1 Ω cm FZ wafer passivated with an optimized SiC_x layer after an in-situ plasma cleaning step.

The injection-dependent lifetime curve measured using QSSPC shows the very high performance of the optimized SiC_x-layers. The effective lifetimes approximate closely the Auger limit as given by the models of Kerr *et al.* [16] and Glunz *et al.* [17], respectively. The surface recombination velocity is well below 5 cm/s for Δn between $1x10^{14}$ cm^{-3} and $1x10^{15}$ cm^{-3}.

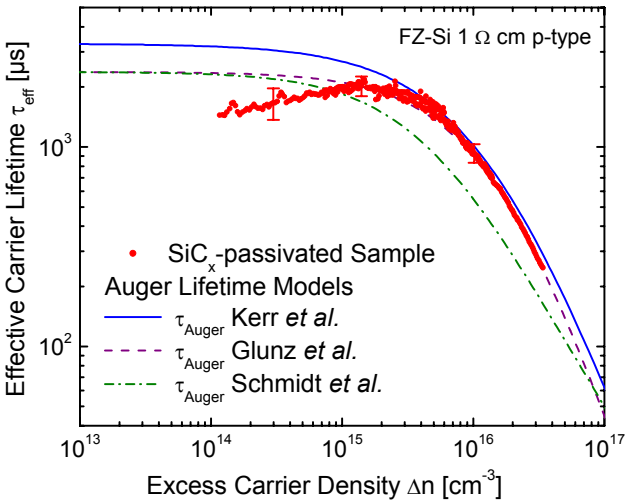

Fig. 3. Effective lifetimes of a 4" 1 Ω cm FZ-Si wafer passivated with SiC_x and three recent Auger lifetime models (Kerr *et al.* [16], Glunz *et al.* [17] and Schmidt *et al.* [18]).

Performance in a solar cell

After the successful development of a highly passivating SiC_x layer, different layer systems based on different compositions were used for the rear passivation of solar cells with a high-efficiency front structure (oxide-passivated 120 Ω/sq emitter and evaporated contacts). Again not only the deposition but also the surface conditioning was performed in the PECVD reactor. E-gun evaporation was used for the deposition of the 2 µm thick Al layer and the laser-fired contacts process was applied. Although the cells have not been annealed after e-gun evaporation and LFC formation, efficiencies greater than 20% have been achieved.

Table 1. Solar cell results with SiC_x rear passivation

Rear surface structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
SiC_x-layer + 2µm Al + LFC	665	37.5	80.3	20.2

The internal reflection of a single SiC_x-layer is already much higher than the one of an Al-BSF (see Fig. 4). This reflection can be significantly increased by applying a second SiC_x layer with a lower refractive index or a PECVD SiO_2 layer.

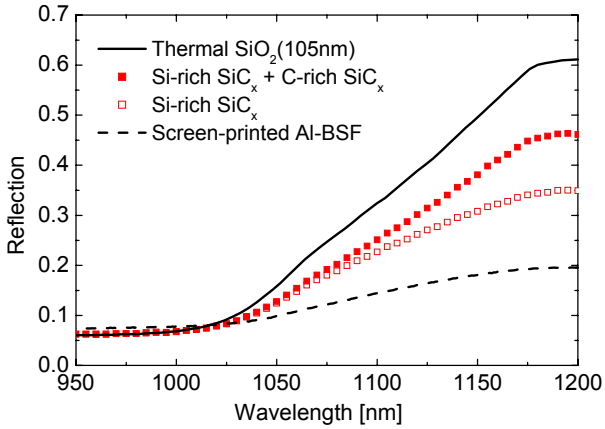

Fig. 4 Reflection of solar cells with different rear surface structures.

Fire stability

The crucial question if the SiC_x layers are fire stable is still open at this point. Thus, we have performed experiments to test if our SiC_x-layers are suited for the process sequence option 2 as displayed in Fig. 1, i.e. the deposition of the passivation layer before the firing step.

In a first experiment we have fired lifetime test samples using 1 Ω cm Fz-Si. The lifetime was measured using QSSPC before and after a firing step without any additional anneal step. The firing step was performed at a peak temperature of 800°C in a standard belt furnace. The chosen temperature of 800°C is lower than in a standard firing step since it was shown that unmetallized samples heat up about 50°C to 80°C higher than metallized solar cells.

Table 2. Carrier lifetime @ $\Delta n = 5x10^{14}$ cm^{-3} of test samples before and after a firing step at 800°C

Layer system	Lifetime before firing [µs]	Lifetime after firing [µs]
LS-08	1126	17.8
LS-10	533	0.8
LS-66	341	250

The measurement results of a few representative layers in Tab. 2 show an interesting finding. The lifetime after deposition is not coupled with the fire stability. The layer system LS-66 which has shown good but not the best passivation quality clearly outperforms its "competitors".

Based on these findings in a second experiment solar cell precursors on 0.5 Ω cm FZ-Si were fabricated with an oxide-passivated 120 Ω/sq emitter and different SiC_x rear passivation layers. In this case the lifetime measured at one sun illumination can be directly translated in the implied open-circuit voltage. Again the structures were measured before and after an 800°C firing step.

Table 3. Implied open-circuit voltage before and after firing step determined from QSSPC measurement at 1 sun on a solar cell precursor. For layer system B the best result and the average of 7 samples after firing is given.

Layer system	max. V_{oc} [mV] before firing step	max. V_{oc} [mV] after firing step
A best result	625	639
B best result	635	679
B average		676 +/- 2.4

Both layer systems shown in Tab. 3 are well suited for the rear surface passivation even after a firing step but especially layer system B is very promising since a very high open-circuit voltage of 679 mV could be obtained.

CONCLUSION

The SiC_x layers and the related in-situ plasma cleaning optimized in this work show a very high passivation quality. Excellent solar cell efficiencies greater than 20% have been achieved. Even more important is the fact that SiC_x layers optimized for thermal stability show an excellent performance after an industrial firing step.

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