IMPACT OF POTENTIAL BARRIERS AT GRAIN BOUNDARIES OF MULTI CRYSTALLINE SILICON WAFERS ON INDUCTIVELY COUPLED RESISTIVITY MEASUREMENTS

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ABSTRACT: Base resistance and emitter sheet resistance are two of the most important process control parameters in solar cell manufacturing, which may be measured inductively. On mono-crystalline silicon, measurement accuracy of this contactless inline technique has already been demonstrated. In this work the investigation of measurement accuracy is extended to multi-crystalline silicon (mc-Si) and reveals for base resistance measurements severe measurement artifacts of up to a factor 2 upon chemical standard treatments, such as damage etching and acidic texturization. The investigation identifies potential barriers at grain boundaries as reason for these artifacts which form upon chemical treatments and further increase with storage time after such chemical steps. It is found that these potential barriers vanish almost completely after thermal treatments, such as a standard emitter diffusion. As a consequence, the emitter sheet resistance calculated from the inductive sheet resistances before and after emitter diffusion may be significantly underestimated if the presumed base resistance is overestimated. Taking into account that mc-Si wafers are almost not affected by potential barriers in the as-cut state, we develop a patented procedure which allows reliable emitter sheet resistance measurements in mc-Si wafers irrespective of the presence of potential barriers before diffusion.

Keywords: Multi crystalline silicon, grain boundaries, sheet resistance, inductive measurement

1 INTRODUCTION

The presence of potential barriers at grain boundaries is already known in semiconductor industry. Special gas sensors, e.g., use the effect of rising potential barriers at grain boundaries for detecting gas concentrations [3]. However, in PV industry potential barriers at grain boundaries are rarely discussed so far. Diaz et al. [4] investigated the electrical activity of grain boundaries in specially grown multi-crystalline Silicon (mc-Si) by monitoring potential barriers at grain boundaries focusing on the impact of different types of grain boundaries on solar cell efficiency.

The present paper investigates potential barriers at grain-boundaries in standard industrial mc-Si focusing on their formation and annihilation upon chemical and thermal treatments which are standard in solar cell processing, such as surface etching and emitter diffusion. Moreover, the impact of such grain boundary barriers on inductive base and emitter sheet resistance measurements is investigated. Both parameters are highly relevant for process control in solar cell manufacturing and can be measured inductively [1]. This contactless measurement principle is inline applicable and allows measurements with high throughput and sufficient spatial resolution. In a recent publication [2], its accuracy and reliability irrespective of the surface morphology has been demonstrated for mono-crystalline Czochralski Silicon (Cz-Si). However, in mc-Si wafers measurement accuracy may be affected by grain boundaries if potential barriers rise, which is investigated in depth here.

As a starting point, some basics on grain boundaries and the inductive measurement principle should be summarized, to give an idea about the expected effects of potential barriers on these measurements. Multi-crystalline wafers typically consist of mono crystalline grains of different crystal orientation and different size which ranges from some square microns to some square centimeter. Since wafers are typically cut from the block vertically to the crystal growth direction, grain boundaries typically penetrate the wafer completely and perpendicular to the wafer surface. Depending on the



Fig. 1 (a) Inductive measurement principle. An alternating magnetic field induces an eddy current in the wafer in a plane parallel to the wafer surface. (b) In mc-Si wafers the eddy current has to pass through grain boundaries and thus may be additionally damped if potential barriers are present, which may distort the measurement results.

crystal growth process, the grain boundary density may vary laterally across the wafer.

As shown in Fig. 1a, the inductive measurement principle is based on an electromagnetic resonant circuit. Bringing a wafer into the narrow air gap of a ferrite core the alternating magnetic field induces an eddy current I_{ec} in the wafer. Since the magnetic flux penetrates the wafer perpendicular to the wafer surface, the eddy current is induced in a plane parallel to the wafer surface. Depending on the number of free carriers in the wafer, the eddy current increases and the resonant circuit is damped according to Lenz's rule. The resulting signal directly correlates to the wafer sheet resistance [1, 2] which thus may be determined. The area in which the eddy current is induced depends on the sensor area and typically is about 1-4 cm², which is bigger than the typical grain size in mc-Si wafers.

Thus, in mc-Si wafers the eddy current has to pass through the grain boundaries. If potential barriers are present at the grain boundaries, the eddy current will be restrained and the measurement signal will be artificially reduced, which is interpreted as a higher sheet resistance than related to the actual doping of the wafer.



Fig. 2 4-point-probe measurement pattern for highresolution resistance mappings of grain boundaries in mc-Si wafers. The pattern consists of 20x20 measurement points in an area of $10x10 \text{ mm}^2$ and is placed on the wafer in a way that a certain grain boundary is covered by the pattern. Orientation of the probe head, with a tip distance of 1 mm, is chosen perpendicular to the investigated grain boundary (see Fig. 3).

Thus, for inductive resistance measurements on mc-Si wafers the following effects are expected and have to be taken into account in signal interpretation. (i) The measured signal does not represent the conductivity of only the grains but a combination of grain conductivity and conductivity over grain boundaries which may differ in the presence of potential barriers. (ii) The influence of potential barriers on the signal does not only depend on the height of the potential barriers but also of the grain boundary density within the wafer area covered by the sensor. (iii) If potential barriers at grain boundaries change with time and/or process-induced, reproducibility of the measurement results may be affected. Moreover, if the emitter sheet resistance is measured inductively and thus calculated from two measurements before and after emitter diffusion [2], the fundamental prerequisite of identical substrate sheet resistances in both measurements may be violated, which may lead to wrong results for the emitter sheet resistance.

To be able to quantify the above mentioned effects on inductive measurements, grain boundaries first have to be investigated with respect to the formation and annihilation of potential barriers.



Fig. 3 Possible alignments of the 4-point-probe tips while crossing the grain boundary. Pos 0: All four probe tips are at one side of the grain boundary. Pos 1: Three probe tips are on one side of the grain boundary while the forth tip is on the other side. Pos 2: Two probe tips are on each side of the grain boundary. Current is impressed from probe tip S1 to S4. Voltage is measured between S2 and S3.



Fig. 4 Line scan of the resistivity values measured by means of the 4-point-probe technique across the grain boundary. The data are extracted from the 20x20 high-resolution map shown in Fig. 2. The position labels describe the alignment of the probe tips to the grain boundary and refer to the definition in Fig. 3. In Pos. 2, when the grain boundary is between probe tip S2 and S3, the measurement signal rises significantly in the presence of a potential barrier.

2 IMPACT OF POTENTIAL BARRIERS AT GRAIN BOUNDARIES ON 4-POINT-PROBE MEASURE-MENTS

The detailed investigation of potential barriers at grain boundaries is done by means of the 4-point probe technique [1] using a specially developed measurement setup. The method used here is a modification of the characterization method from Diaz et al. [4] who used the Wenner method instead of the Van der Pauw method for the resistance measurements. For the measurements we use a TC150 probe head from Jandel with a distance between each of the 4 probe tips of 1 mm. As shown in Fig. 3, current is impressed from probe tip S1 to probe tip S4 while voltage is measured between probe tip S2 and S3. For grain boundary characterization a high resolution mapping is performed using a raster of 20x20 measurement points in an area of $10 \times 10 \text{ mm}^2$ leading to a resolution of 500 µm in both directions. The wafer is positioned under the probe head in a way that the grain boundary of interest crosses the measurement raster horizontally (see Fig. 2) and that the 4 linearly arranged probe tips of the probe head are aligned perpendicular to the grain boundary (see Fig. 3). This orientation ensures that by measuring the whole raster the probe head steps over the grain boundary several times while moving from on grain to the other as displayed schematically in Fig. 3.

For the alignment of the probe tips to the grain boundary, three different constellations are possible (see Fig. 3). The resulting resistivity signal in the different constellations is shown in Fig. 4 by an exemplary resistivity line scan for a grain boundary with potential barrier. (Pos. 0) All 4 probe tips contact the same grain. Existing potential barriers at the grain boundary have almost no impact on the measurement result. The measured resistivity reflects the actual doping of the wafer. (Pos. 1) One probe tip contacts the grain on one side of the grain boundary, the other three probe tips contact the grain on the other side. In this constellation a potential barrier induces an additional voltage drop between sensors S1 and S2 but does not lead to a voltage increase between sensors S2 and S3 and thus not to an increased resistivity. In contrast a slight resistivity decrease is observed in this constellation which may



Fig. 5 High resolution resistivity topography of a grain boundary measured by means of the 4-point probe technique using the setup shown in Fig. 2 and Fig. 3. (a) In the as-cut state the potential barrier at the grain boundary is detectable but negligibly small. (b) After wet chemical etching strong potential barriers are formed, the measured specific resistivity varying between 1 Ω cm near the grain boundary and up to 15 Ω cm across the grain boundary.

originate from a barrier-induced widening of the measurement current path between sensors S2 and S3 which itself may lead to a slight voltage drop between S2 and S3. (Pos. 2) Each of the two neighboring grains is contacted by two probe tips the grain boundary being inbetween sensor S2 and S3. In the presence of a potential barrier, the voltage drop between Sensor S2 and S3 increases significantly and results in a significant resistivity increase, which can be used as an indicator for the potential barrier. It is obvious that the gained resistivity results for the grain boundary do not reflect absolute resistivity values but only relative ones as the measured specific resistivity is defined for a homogeneous 3dimensional volume and not for a 2-dimensional plane which the grain boundary represents. However, this does not affect the informative value of the measured quantity. The special constellation, where one of the probe tips contacts the grain boundary itself is undetermined and not recognized any more.

Since the wafer can be repositioned on the measurement chuck with an accuracy of less than 1 mm, it is possible to re-measure the same grain boundary several times, e.g., after different process steps. Fig. 5 exemplary shows two resistance topographies of a grain boundary measured by means of the procedure described above in two different states. In the as-cut state (see Fig. 5(a)) the grain boundary is clearly visible but the height of the potential barrier is very low. After wet chemical texturization (see Fig. 5(b)) the same grain boundary shows a significantly increased potential barrier which is reflected in a resistivity increase from 1 Ω cm near the grain boundary to 15 Ω cm across the grain boundary.

3 IMPACT OF POTENTIAL BARRIERS AT GRAIN BOUNDARIES ON INDUCTIVE RESISTANCE MEASUREMENTS

The inductive sheet resistance measurements are performed with the inline measurement device PV-RT 2001 from KITEC company (see Ref. [2]). The system uses 3 inductive sensor pairs which are arranged in a line perpendicular to the transport direction. The sensor pairs have a diameter of 25 mm and an air gap of 3 mm inbetween the two sensors. As the wafer is measured "onthe-fly" (i.e., while being moved by the conveyor belt through the sensor gap with constant velocity), the sheet resistance is measured spatially resolved in transport direction along three traces. As each sensor collects data every 17 ms, about 50 data points are collected from each sensor for a wafer with an edge length of 156 mm if the conveyor belt speed amounts to 150 mm/s.

As an example, Fig. 6 displays a typical inductive data set showing the base resistance of a mc-Si wafer along three traces as a function of wafer position. The open symbols show the base resistance values as they are expected from the barrier-free base resistance measurement in the as-cut state, the slight resistivity increase due to material ablation during etching being taken into account by a thickness correction factor (see section 5). As can be seen, the measured values deviate from the expected values by 6-12% to higher values. This slight resistance increase is a measurement artifact which has to be attributed to a slight formation of potential barriers at the grain boundaries due to the chemical treatment as will be proved in the next section. Fig. 7 shows a similar data set after damage etching. As can be seen, the measured values (closed symbols) are increased by more than a factor 2 compared to the expected values (open symbols). This strong increase and the strong variations across the wafer are originated from a strong formation of potential barriers due to the chemical treatment, as will be shown in the next section. Due to the steep slopes of the resistance values the resistance measurements become impossible on two of the three data traces. This demonstrates the strong impact of the effect. The reduction of the measurement signal which is interpreted as a sheet resistance increase is caused by an inhibited flow of the eddy current in presence of potential barriers at grain boundaries. Since the sensor area is about 5 cm^2 both, grain boundary density and potential barrier height contribute to the effect. The strong variations across the wafer, which are observed in Fig. 6 and especially in Fig. 7, may be explained by variations in the grain boundary density across the wafer whereas the potential barrier height is assumed to be constant over



Fig. 6 Base sheet resistance of a mc-Si wafer (with 156 mm edge length) measured inductively along three traces as a function of wafer position. Slight measurement artifacts are observed after acidic etching. (**Top**) Sheet resistance as it is expected from the measurements before the chemical treatment (open symbols) in comparison to the sheet resistance effectively measured after the chemical treatment (closed symbols). (**Bottom**) Relative deviation of the effectively measured from the expected value which ranges here between 5-13%.



Fig. 7 Base sheet resistance of a mc-Si wafer (with 156 mm edge length) measured inductively along three traces as a function of wafer position. Strong measurement artifacts are observed after alkaline damage etching. **(Top)** Sheet resistance as it is expected from the measurements before the chemical treatment (open symbols) in comparison to the sheet resistance effectively measured after the chemical treatment (closed symbols). **(Bottom)** Relative deviation of the effectively measured from the expected value which ranges here up to 200 %.

the wafer though variations cannot be excluded.

4 PROCESS-INDUCED FORMATION OF POTEN-TIAL BARRIERS AT GRAIN BOUNDARIES

In order to evaluate the process impact on the formation of potential barriers at grain boundaries, neighboring wafers of one mc-Si material have been subjected to different chemical standard processes. All samples have been investigated by means of inductive resistance measurements and high-resolution 4-point-probe measurements, to be able to prove correlations of artifacts in the inductive measurements with potential barriers. For reasons of comparability, the 4-point-probe resistance topography has been measured at the same grain boundary in all wafers.

The following processes have been applied: (i) The first wafer has been measured in the as-cut state and represents the reference value. (ii) The second wafer has been measured immediately after the damage etching, rinsing in DI-water and drying under a nitrogen flow. (iii) The third wafer has been subjected to the same procedure as the second wafer but has been measured only after 24 hours storage under lab atmosphere. (iv) The fourth wafer has been damage-etched and rinsed in the same manner as before but was dried with a hot air dryer and has again been measured only after 24 hours storage under lab atmosphere.

The measurement results are displayed in Fig. 8. As can be seen, the potential barriers are already visible but not significant in the as-cut state (see Fig. 8a). Immediately after the damage-etching step the potential barriers slightly increase to about 5 Ω cm from about 2 Ω cm in the as-cut state, which is reflected in an increase of the inductively measured sheet resistance by about 10 Ω /sq (see Fig. 8b). After an additional storage for 24 hours under lab atmosphere the inductively measured sheet resistance further increases significantly by about 25 Ω /sq compared to the as-cut value (see (Fig. 8(c1)). A closer look at the 4-point-probe topography reveals that only the increase of the potential



Fig. 8 Process- and time-dependent formation of potential barriers at grain boundaries in mc-Si wafers and their impact on inductive resistance measurements: (**right**) 4-point-probe resistance topography of an individual grain boundary, (**left**) inductive resistance measurement across the whole wafer (symbols) in comparison to the as-cut measurement (lines). Potential barriers and measurement artifacts (a) are negligible in the as-cut state and increase significantly upon (b) etching, (c) air storage and (d) air drying.

barrier height to about 7 Ω cm is responsible for the observed increase of the inductively measured base resistance as the base resistivity in the grains remains unchanged (see Fig. 8(c2)). If the wafer is dried with hot air instead of nitrogen, the potential barriers rise even stronger reaching barrier heights of 19 Ω cm (see Fig. 8(d2)). These barriers lead to inductive resistance measurements which vary strongly across the wafer and are increased by more than a factor 2 compared to the expected value related to the base doping (see Fig. 8(d1)).

The process variation shows that the formation of potential barriers at grain boundaries is easily initiated by chemical treatments, sensitively reacts to the precise process implementation and is favored by time. Moreover, it turns out that inductive base resistance measurements are very liable to barrier-induced measurement artifacts after etching.

Additional investigations which will be published elsewhere [5] prove that potential barriers are annihilated by thermal processes, such as the emitter diffusion, and thus most likely do not affect the final cell. However, they strongly affect inductive emitter sheet resistance measurements, which is highly relevant for process control reasons and will be discussed in the last section.

5 MEASUREMENT PROCEDURE FOR RELIABLE INDUCTIVE EMITTER SHEET RESISTANCE MEASUREMENTS FOR MC-SI WAFERS

If the emitter sheet resistance $R_{emitter}$ is measured inductively, it has to be calculated from the substrate sheet resistance R_{basis} measured before emitter diffusion and the parallel sheet resistance of basis and emitter $R_{parallel}$ measured after emitter diffusion. For a doublesided emitter the conditional equation is derived as [2]:

$$R_{emitter} = 2 \times \frac{R_{basis} \times R_{parallel}}{R_{basis} - R_{parallel}}$$
 Eq. 1

In the case of single-sided diffusion the above equation has to be divided by the factor 2.

The equation is only valid, if the substrate sheet resistance R_{basis} is well known and identical in both measurements. Typically, R_{basis} is measured just after surface etching and before emitter diffusion as the sample thickness then remains unchanged. However, in the case of mc silicon where potential barriers are likely to be present at grain boundaries before diffusion and vanish after diffusion, the fundamental prerequisite of identical substrate resistance may easily be violated. Thus, the substrate resistance R_{basis} routinely measured before diffusion cannot be used for Eq. 1.

By experience, grain boundaries are not affected by significant potential barriers in the as-cut state, which is thus a suitable state to determine the actual basis sheet resistance reliably. To be able to use this value in Eq. 1 a correction has to be applied which accounts for the thickness ablation due to the etching step. This is done by the following simple equation

$$R_{basis_correct} = R_{basis_ascut} \times \frac{d_{ascut}}{d_{after_etch}}$$
 Eq. 2

where $R_{basis_correct}$ is the thickness-corrected basis sheet resistance, R_{basis_ascut} the basis sheet resistance in the ascut state, d_{ascut} the wafer thickness in the as-cut state and d_{after_etch} the wafer thickness after the etching process.

Using $R_{basis_correct}$ from Eq. 2 in Eq. 1, the inductive measurement technique is also applicable for reliable emitter sheet resistance measurements on mc-Si wafers, which is a patented procedure [6].

The relevance of this procedure is demonstrated in Fig. 9 for a double-sided emitter diffusion. The simulated curves show the relative error of the emitter sheet resistance, derived from Eq. 1 by error propagation, as a function of (i) the measurement error of substrate sheet resistance and (ii) the ratio of the emitter and substrate sheet resistance. As expected the emitter error increases with increasing substrate error. This increase is the stronger the higher the ratio of emitter and substrate sheet resistance, i.e., the smaller the difference between parallel



Fig. 9 Error of the emitter sheet resistance, calculated from the substrate and parallel resistance according to Eq. 1, as a function of the barrier-induced measurement error of the substrate sheet resistance for different ratios of the emitter and the substrate sheet resistance. The simulations are valid for a double-sided emitter diffusion.

and substrate sheet resistance. Thus, the emitter errors become the highest for lowly doped high-efficiency emitters and highly doped substrates. For a typical wafer thickness of 200 µm and a typical specific substrate resistivity in the range from 0.5 to 2.0 Ω cm, the substrate sheet resistance ranges from 25 to 100 Ω /sq. Assuming a wafer with 1 Ω cm (50 Ω /sq.) substrate resistance and an industrial emitter with 50 Ω/sq. (emitter/substrate ratio = 1), the emitter sheet resistance is underestimated by about -7% (or $3.5 \Omega/sq.$) if a moderate error of 20% is assumed for the error of the substrate resistance. For high-efficiency emitter with 100 Ω /sq. (emitter/base ratio = 2) the emitter sheet resistance is already underestimated by about -15% (or 15 Ω /sq.). As the trend goes to lowly doped emitters and as the barrier-induced measurement error of the substrate resistivity may be much higher, these examples demonstrate the necessity to apply the patented procedure to ensure a reliable process control in the presence of potential barriers.

6 CONCLUSION

Investigating measurement accuracy of inductive base and emitter sheet resistance measurements on standard industrial mc-Si wafers, the present study reveals severe measurement artifacts after standard etching processes. The detailed analysis of grain boundaries by means of specially developed high-resolution resistance scanning using the 4-point-probe technique reveals that these artifacts have to be attributed to potential barriers which arise at grain boundaries upon chemical etching processes such as alkaline damage etching and acidic texturization. It is found that the barrier height increases further with storage time. As these potential barriers inhibit the lateral current in eddy currents, the inductively measured base sheet resistance may increase artificially by more than a factor 2.

Moreover, it is found that the potential barriers vanish after high-temperature processes, such as emitter diffusion, and thus do not affect the final cell. However, it strongly affects the inductive determination of the emitter sheet resistance which is based on a two-step measurement before and after diffusion. In contrast to the barrier-induced measurement error on the substrate sheet resistance, the calculated emitter sheet resistance may be significantly underestimated if the presumed base sheet resistance is overestimated. Since this effect directly correlates to the grain boundaries in the wafer, its relevance increases with the density of grain boundaries.

However, the investigations on mc-Si wafers show that the effect of potential barriers at grain boundaries is almost irrelevant in the as-cut stage of the wafers. That is why it is strictly recommended to perform inductive resistivity measurements of the substrate before any chemical treatment. In the case of emitter sheet resistance measurements, material abrasion during the chemical treatment requires an additional thickness correction of the measured substrate values in the as-cut state to provide correct values for the emitter sheet resistance. Applying the patented procedure, inductive measurements allow reliable process control of the emitter diffusion process even for barrier-affected mc-Si wafers.

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