SOLAR CELL PROCESSING OF RECRYSTALLIZED WAFER EQUIVALENTS ON LOW-COST CERAMICS

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ABSTRACT: As the material cost make around one third of the cell costs a crystalline silicon thin-film technology like ours is very attractive. It combines the advantages of crystalline Si (processing experiences, no degradation, high acceptance in public), a thin-film technology (lower material and energy costs) and attractive cell process and module alternatives (e.g. integrated back surface field and optical confinement, interconnected grid, shingle technology). In this publication we will discuss principle challenges in wafer equivalent processing. Latest progresses concerning breakage rate, throughput and optimized processing will be presented. Furthermore solar cell processing and occurring problems will be discussed. Solar cell results on 21 cm^2 with efficiencies of 5.9% before anti-reflection coating will be presented.

Keywords: thin film solar cell, ceramic substrate, SiC

1 INTRODUCTION

In our Recrytallized Wafer Equivalent (RexWE) [1] we aim to imitate the most positive features of a standard wafer, like high-efficiency potential, modularity and mechanical strength. To achieve this, we create a thin c-Si layer on top of a SiC capped foreign substrate, in this paper we discuss the use of RBSiC ceramics. Unlike a wafer the steps “wafer manufacturing” and “solar cell processing” cannot be described as two distinct process parts for RexWE. Starting with the deposition of the SiC layer we work on the optical confinement of the thin-film cell and by depositing the highly doped seeding layer we already create a back surface field (BSF). This means for the wafer equivalent, that the rear-side of the cell is located (and protected) inside the WE (see Fig. 3). At the beginning of this paper we will focus on the progress made in realizing a RexWE and will afterwards proceed with the challenges during solar cell processing.

2 WAFER EQUIVALENT PROCESSING

2.1 Silicon deposition

Because many of our processes are realized in optically heated furnaces (silicon deposition and recrystallization) the absorption of the substrate plays an important role. In comparison to the silicon wafer, which can also be used as a substrate, the reaction bonded SiC ceramics (RBSiC) absorbs much more of the irradiated energy from the halogen lamps. The growth rate of the silicon seeding layer (at 960°C) was therefore much higher (1.3-2.0 times) on RBSiC ceramics. Additionally, the differences in thermal mass and conductivity made process adaptations necessary. The rough surface of the substrates, still present though SiC capped, was another parameter which influenced the silicon growth process. Nevertheless, after considering all these specific features, the layer quality seemed to be as good as on silicon substrates. The low amount of whiskers and the good recrystallization results confirmed this impression.

2.2 Breakage rate

The breakage rate during high temperature processes (CVD, ZMR) was extremely dependent on the sintering atmosphere and sintering sequences (gas, vacuum) during ceramic production. Besides that, adaptations in wafer equivalent processing significantly decreased breakage rate:
(1) Because many cracks started from the ceramic edges laser cutting was suspected to have a negative influence on the substrates integrity (defect generation due to very fast heating and cooling). To avoid the laser cutting we punched the green tapes directly into the proper dimensions. (2) Cracking frequently occurs during silicon deposition. We could trace this problem back to improper settings of the controller circuit, which led to too high temperature gradients. A soft start program almost completely solved this problem. (3) The zone melting recrystallization (ZMR) process caused the highest breakage rate. Temperature gradients due to melting lamp, radiation losses on the substrates edges and the cold process gases (room temperature) were suspected to cause tensions, curvature and in worst case cracking. By an optimized profiling of the large area heater (separate lampfield zones) radiation losses could be regulated. The power for the melting zone itself was chosen to be as low as possible for low temperature gradients from rear- to front-side of the substrates. These efforts resulted in a much lower breakage rate and less bowing of the wafer equivalents. Simulations done by University of Erlangen (Germany) showed, that a preheating of the process gas could further reduce internal tensions and curvature.

2.3 Recrystallization speed and thermal capping

During optimization of the recrystallization parameters with respect to scan speed and layer quality, we could observe some beneficial effects of the SiC diffusion barrier. The wetting effect of liquid silicon on SiC barrier layer seemed to be much better than on SiO_2. Because of the liquid silicon’s tendency to drop formation an oxide capping layer is necessary. The enhanced wetting effect enabled us to reduce the capping layer thickness significantly. Therefore, to further enhance throughput and effectiveness of the recrystallization process, we tried to use thermal capping as an alternative to plasma deposited SiO_2. At 1250°C, 100 nm of thermal oxide in pure O_2 atmosphere were grown in-situ for 10 min. In Fig. 1 one can find micrographs of the melting zones during recrystallization

at 10 (left), 50 (middle) and 100 mm/min. All three graphs show homogeneous melting zones, with no balling-up effects at all. The zones of molten silicon became wider with increasing scan speed. At the one sample recrystallized at 100 mm/min one can observe extremely large facets. This was caused by a "super cooled" zone, where the liquid silicon had temperatures below 1414°C.

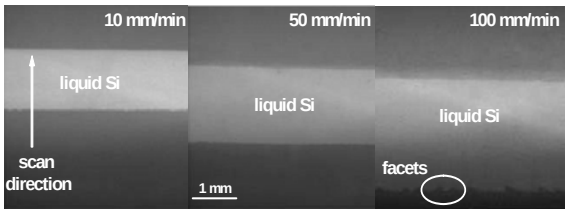

Fig. 1: Melting zones (bright) and facet growth at the solidification front of Si on RBSiC with SiC layer recrystallized with 10 (left), 50 (middle) and 100 mm/min (right).

After removing the thermal oxide with hydrofluoric acid (HF, 50%) we etched the substrates in hot KOH to make the silicon grains visible. Fig. 2 shows micrographs of the recrystallized silicon layers. As expected from the observations during zone melting the sample recrystallized at 100 mm/min had the largest grains.

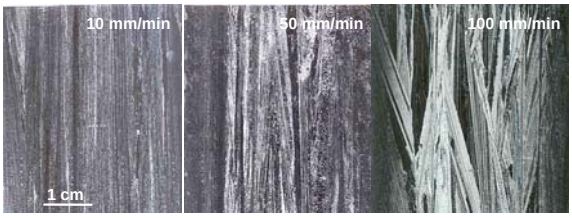

Fig. 2: Micrographs of silicon layers capped with thermal oxide and recrystallized at 10 (left), 50 (middle) and 100 mm/min (right).

These results proved, that 100 nm of thermal capping layer thickness are sufficient to realize good crystallization processes. Additionally an increased scan speed leads to larger grains. For the throughput of our process these two results mean an enormous enhancement.

2.4 Further improvements in RexWE processing

One important cost factor for the wafer equivalent production is the SiC diffusion barrier layer. To minimize these costs we tried to make the SiC layers as thin as possible without degrading diffusion barrier performance. Therefore, the SiC diffusion barrier layer thicknesses were reduced to 300 nm (standard thickness 1000 nm). The seeding layers grown on the thin SiC layers showed as good quality as on thick layers (no whisker growth). During recrystallization no different behaviour was observed and the recrystallized silicon layers show no difference in grain size.

Simulations showed [2], that 5 µm of a highly doped ($3x10^{18}$ cm^{-3}) silicon seeding layer, when calculating with minority carrier lifetimes of around 10 to 30 µs, is the optimum thickness to create a good back surface field (BSF). Therefore we varied the thickness of the seeding layer, which later serves as BSF. Due to the substrates roughness and its open porosity a certain amount of the silicon seeding layer drains into the ceramic substrate during ZMR. Though SiC prevents a direct contact between liquid silicon and RBSiC grains, the pores are not completely capped with the diffusion barrier layer. We tested seeding layers with thicknesses of 10 to 15 µm. The 10 µm thin layers could not be recrystallized successfully. The 15 µm thick ones reduced to 8-10 µm after ZMR and showed large grains. The achieved BSF layer is therefore still thicker than optimum. Without reduction of the open porosity the recrystallization of thinner silicon layer seems to be quite challenging from today's view.

The optimum thickness for the epitaxial bulk layer has also been simulated [3]. The results show, that an optimum thickness between 10 to 15 µm seems to be desirable. Considering a loss of 5 µm for the (not yet optimized) texturization process (see chapter 3.1) we deposited 20 µm. The doping gas flow (B_2H_6) was slightly decreased from the beginning to the end of the process. The resulting gradient doping profile ($1x10^{17}$ to $1x10^{16}$ cm^{-3}) should enhance J_{sc} ("drift field" effect).

3 SOLAR CELL PROCESSING

Though the RexWEs are crystalline silicon wafer equivalents not all standard solar cell processes applied on silicon wafers can be transferred directly. In this chapter we will give an overview on tested solar cell processes, will discuss occurring challenges and show the progress already achieved. In principle the porous substrate structure is in favour of "dry" processes, but wet chemical processing is also possible when applying intense rinsing or when working with one side etching processes. The suitable equipment for high throughput applications is already available and is becoming more and more important in industrial silicon solar cell processing.

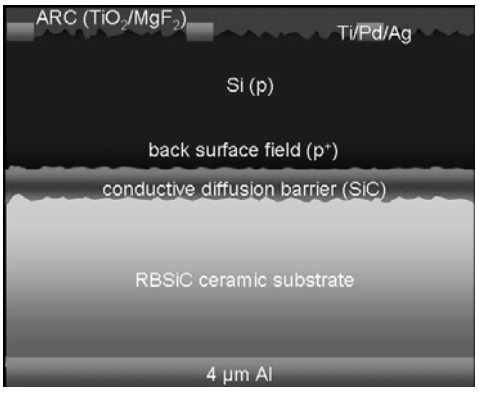

Fig. 3: Solar cell processed on a recrystallized wafer equivalent (RexWE) with integrated back surface field (BSF) and diffuse Bragg reflector.

3.1 Texturization with KOH and plasma

Especially thin solar cells need a good optical confinement to absorb the whole irradiated spectrum of light. This includes, beside an anti-reflection coating, a texturized front side and a diffuse Bragg reflector at the cell's rear side. Different texturization processes were tested in application to the RexWE. Two texturized surfaces are shown in Fig 4. On the left hand side a partly plasma etched one, with very small pyramids can be found. To point out the difference between a texturized

and an untexturized surface half of the sample was capped with a protection layer during etching with SF_6. It can be clearly seen, that all grains are homogeneously textured (reflection ≈20%). The silicon removal was around 4 µm. The right micrograph shows the textured surface which was wet chemically processed with 85°C hot KOH/IPA for several minutes. Due to the anisotropic etching behaviour of KOH the random "pyramids" look different from grain to grain. Only grains with <100> surface have random pyramids. The silicon surfaces of the sample in Fig. 4 were obviously tilted relative to <100>. Therefore the random pyramids were etched diagonal out of the silicon.

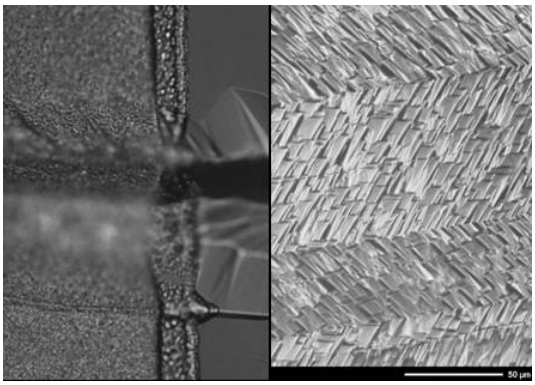

Fig. 4: Micrograph of a partly plasma (left) and a KOH (right) texturization on a recrystallized wafer equivalent surface.

3.2 Phosphorous emitters on RBSiC

To compare different grid structures we tested emitters between 80 and 120 Ω/sq.. For contacts fully evaporated through shadow masks 80 Ω/sq. emitters were used. Because here the process does not allow a passivation of the surface a higher doping level to lower the surface recombination velocity was chosen. The photolithographic front grids were applied on 120 Ω/sq. emitters. Here the emitter surface was passivated with a 10 nm thin oxide. This was also necessary to avoid problems during electroplating. Without the thin oxide layer parasitic depositions of Ag on silicon tips of the rough surface could appear. The emitters were diffused in a tube furnace with $POCl_3$. Measurements with emission sheet resistance imaging [4] (SRI) on the silicon references showed good homogeneities of all emitters. Unfortunately no measurements, not even with a 4-point-tool, were possible on the RexWEs. Crystallinity (lateral conductivity dependent on grain boundaries) and surface roughness influenced the measurements and made an interpretation almost impossible. Measurements with secondary ion mass spectroscopy (SIMS) neither seemed promising, because the always rough surface would make a good depth resolution impossible. Because the emitter furnace was heated with a resistance heater optical absorption should have no influence on the temperature on the samples substrate. Therefore we concluded that the emitters should not be that different on silicon wafer and wafer equivalent.

The most challenging problem during solar cell processing was the phosphorous glass removal. Depending on etch solution, a more or less pronounced colouring of the surface could be observed. Nevertheless, the parasitic layer, though invisible below around 10 nm thickness, could never be completely removed. All attempts trying to identify the composition or the origin of this layer were not successful yet. Due to excellent solar cell results on the silicon references (one at the beginning and one at the end of the tube) a cross contamination during emitter diffusion could be excluded. Cross contaminations during wet chemical processing or drying could be excluded with the same argumentation.

3.3 Front grid deposition

As already mentioned above we tested different grid designs and deposition methods on our RexWEs. Fig. 5 (left) shows the photolithographic grid for high efficiency solar cells. Due to surface roughness and curvature of the substrate the too small grid fingers were often intercepted. On solar cell areas of 21 cm^2 several cells with these interceptions could be found. Though the substrate curvature could be reduced significantly throughout our experiments this was still one of our major challenges.

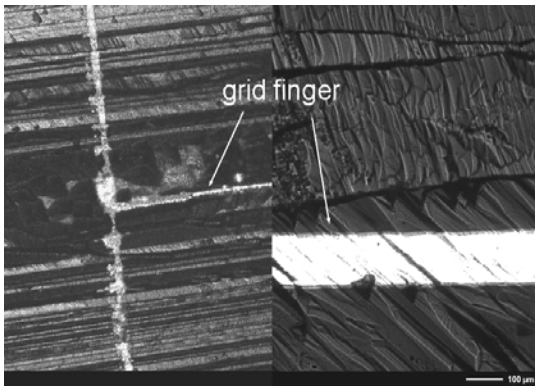

Fig. 5: Photolithographic (left) and evaporated front grid on RexWE solar cell surface

The evaporated grid (30/30/5000 nm of Ti/Pd/Ag) had very broad fingers which adhered quite well to the cell surface. Of course the shadowing effect of this grid was very high (see Fig 5, right micrograph). One solar cell with an evaporated grid was additionally electroplated. Though no parasitic depositions could be observed the cell performance did not change. There seemed to be no current limitation coming from the grid finger's series resistance.

3.4 Remote plasma hydrogen passivation

Because the recrystallized silicon layers had relatively high defect concentrations (especially in the epitaxial layer) a bulk passivation with remote plasma hydrogen passivation (RPHP) was necessary. After 30 min at 350°C the best V_{oc} increased from 532 to 545 mV. Compared to earlier results on other ceramic substrates, this enhancement of 13 mV is only 1/3rd of the "usual" value, probably due to a not yet optimized process.

3.5 Anti reflection coating

The effect of layer residuals after phosphorous glass removal had detrimental impact on the TiO_2/MgF_2 anti-reflection coating (ARC). Because both RexWE solar cell types had undefined layer residuals the ARC

thickness could not be adjusted. The cell performance therefore was even worse after ARC deposition (see Table 1). Fig. 6 shows a micrograph of the solar cell surface after ARC with the unidentified layer residuals.

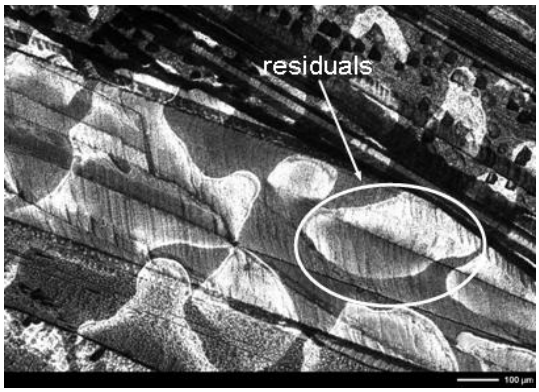

Fig. 6: In homogeneities of the anti-reflection coating due to layer residuals (brighter areas).

3.6 Transfer to large cell areas

Because the fabrication of large area wafer equivalent up to 200x200 mm^2 was already demonstrated [1] and the diffusion barrier performance of SiC (on large areas) had to be investigated we also enlarged the solar cell area. All solar cell processing results explained so far were achieved on a solar cell area of 21 cm^2 (first solar cells on this area). The most important difference to processing of 1 cm^2 solar cells was, as already mentioned above, the curvature of the substrates. Due to grid interceptions and the residual layers on the surface, the best cell with a photolithographic grid achieved only an efficiency of 1.9% with V_{oc}=470 mV and J_{sc}=14 mA/cm^2 (*FF*=29%). The comparison with the reference cell on FZ silicon processed in the same batch (η=16.9%, V_{oc}=640 mV, J_{sc}=34 mA/cm^2, *FF*=78%) showed, that the process itself has high efficiency potential and that cross contamination is not an issue.

Table 1: Solar cell (21 cm^2) results achieved on RexWE on RBSiC substrate measured after front grid deposition, hydrogen passivation (RPHP) and anti reflection coating (ARC).

cell status	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]
front contact	532	18.4	55.2	5.4
RPHP	545	18.8	57.9	5.9
ARC	543	18.9	56.2	5.8

The results for the best solar cell with an evaporated grid design can be found in Table 1. Considering all occurring problems during cell processing, the uniqueness of the cell (first cell on such area) and the missing ARC the efficiency of 5.9% is encouraging. The low fill factor (FF) reflects the series resistance problems most probably caused by the residual layer on the cell surface. Relatively high V_{oc} values were another proof [1] for the good diffusion barrier performance of SiC. The best FZ reference cell (η=9.8%, V_{oc}=608 mV, J_{sc}=22.3 mA/cm2, *FF*=72%, before ARC) showed the high shadowing effect of the evaporated grid and the need for an enhanced texturization process.

4 CONCLUSIONS AND OUTLOOK

In this publication we presented progress in the RexWE processing on a low-cost RBSiC ceramic. The breakage rate could be reduced due to an optimized silicon deposition and recrystallization processing. With the use of a thin, in-situ grown, thermal capping oxide and an increased scan speed (ZMR) of 100 mm/min the throughput was enhance by a factor of 10 compared to the standard process. The SiC layer thickness could be reduced from 1000 nm to 300 nm and led to comparable silicon layer qualities still. Occurring challenges during solar cell processing like texturization, phosphorous emitter formation and grid deposition have been discussed. There is still a lot of potential for cell process improvement. Problems with residual layers after glass removal have to be solved to achieve satisfying fill factors. Nevertheless, the solar cell results with 5.9% efficiency on 21 cm^2 before anti reflection coating, on a real low-cost substrate with a conductive SiC diffusion barrier, encourage our efforts to realize better crystalline thin-film solar cells.

5 ACKNOWLEDGEMENTS

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