TSV-BASED PASSIVE NETWORKS FOR MONOLITHIC INTEGRATION IN SMARTPOWER ICS FOR AUTOMOTIVE APPLICATIONS

Fraunhofer Institute for Integrated Systems and Device Technology IISB

2019-03-13

T. ERLBACHER, G. RATTMANN

10. GMM FACHTAGUNG: AUTOMOTIVE MEETS ELECTRONICS 2019, 12./13.03.2019, DORTMUND, GERMANY

Content

- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

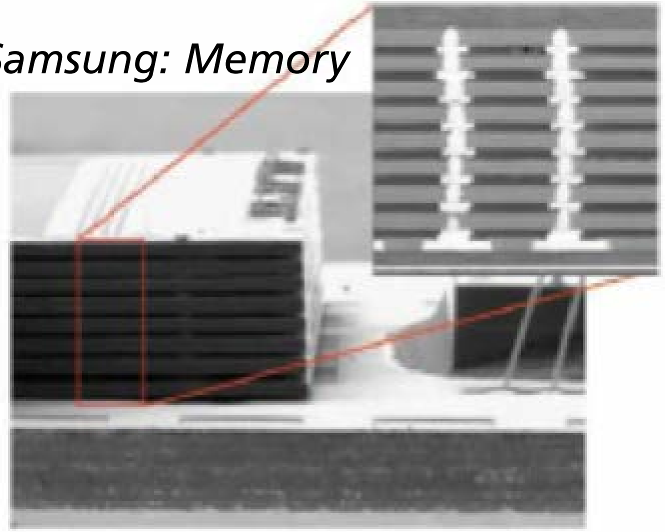
Content

- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

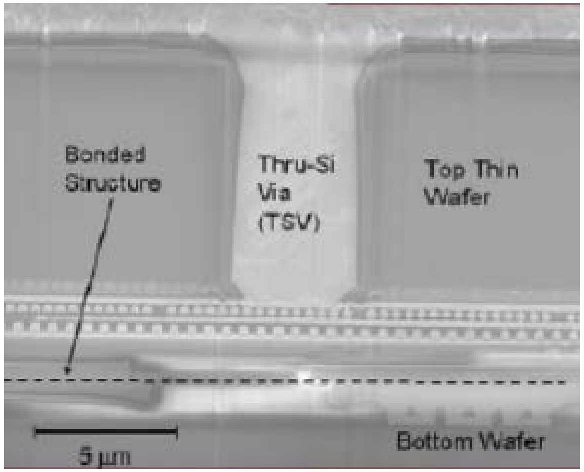
Motivation: 3D integration of power electronics

- Minimization of interconnection through Silicon interposers and 3D stacking
  - Better electrical performance
  - Lower power consumption
  - Wider data width and thus bandwidth
  - Higher density
  - Smaller size
  - Lighter weight
  - Lower cost (hopefully)

Samsung: Memory



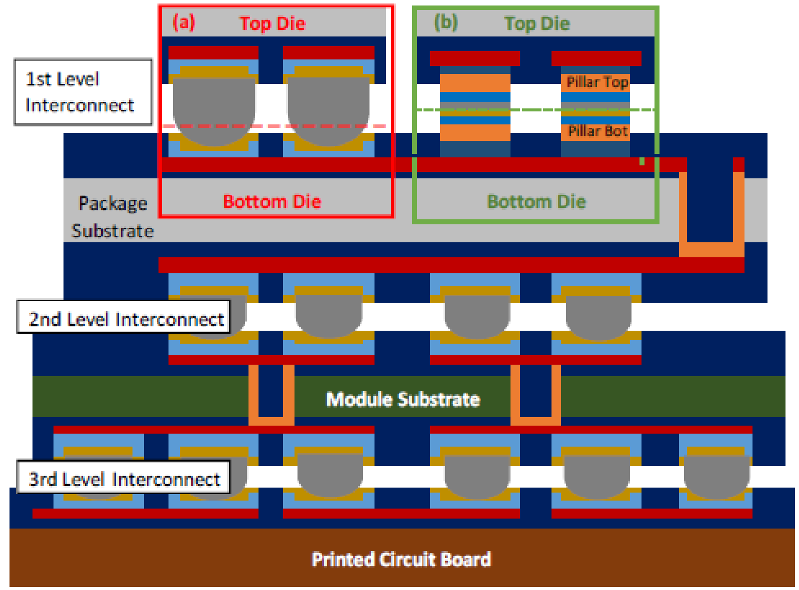
Intel: CPU



- More-than-Moore integration
  - High switching frequencies (several MHz) enable capacitive DC-DC converter designs

Motivation: 3D integration of power electronics

- 3D integration is also feasible for power converter topologies
  - Reduction of parasitic inductances
  - Reduction of coupling capacitances
  - → Fast switching (smaller systems)

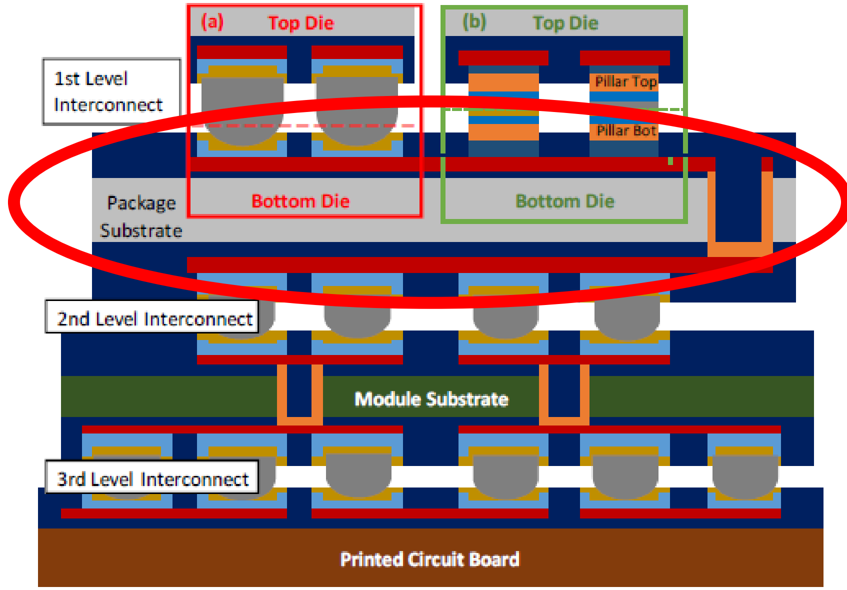


Wachmann et al. (AMS), DATE 2016

- Extension of ASIC processing required
  - CMOS technology
  - + High-voltage devices (e.g. 48V)
  - + TSV-technology for 3D stacking
  - **+ Integrated capacitors**
    - → Extended platform technology
    - High volume required (to work the economy of scales): <u>Demonstration</u> for EV / HEV Automotive applications

Motivation: 3D integration of power electronics

- Demonstration for EV / HEV Automotive applications
  - Technology for Silicon interposer
    - with integrated passive devices
    - with power devices
    - TSV / CMOS compatible fabrication process
  - Integration density for capacitance
  - Overall device performance
  - Work-bench testing of devices in target application:
    - 48V DC-DC converter



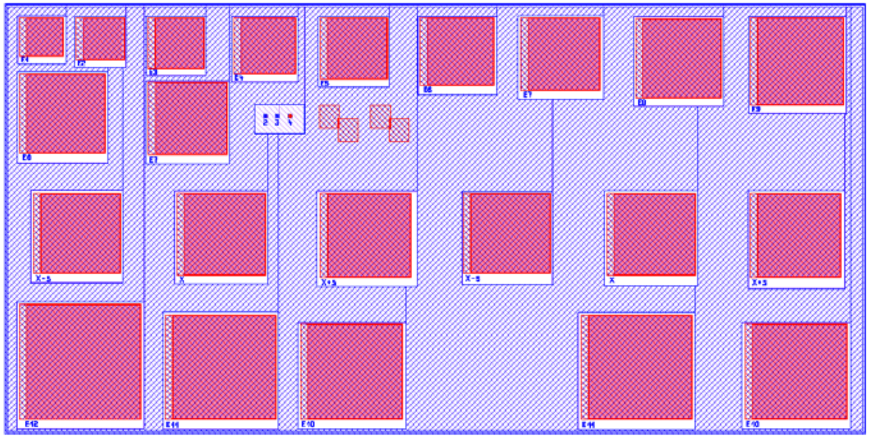
Wachmann et al. (AMS), DATE 2016

Content

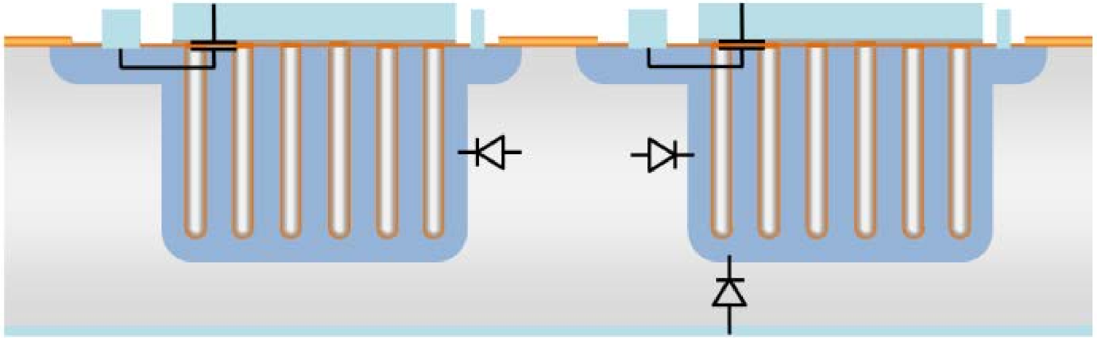
- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

Design of integrated lateral capacitors and diodes

- Design goals:
  - Compatibility of CMOS processing (including TSV)
  - High integration density
    → Trench patterns for area enlargement (A* = 10-15)
  - Multiple capacitors on one chip
    - Junction isolation with n-well in p-substrate
    - Demonstration through **E12** series
  - Low ESR
    → Highly doped trench regions



Mask design



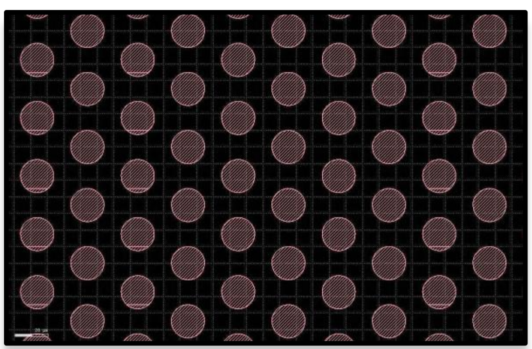
Schematic cross-section

T. Erlbacher, 08.11.2018

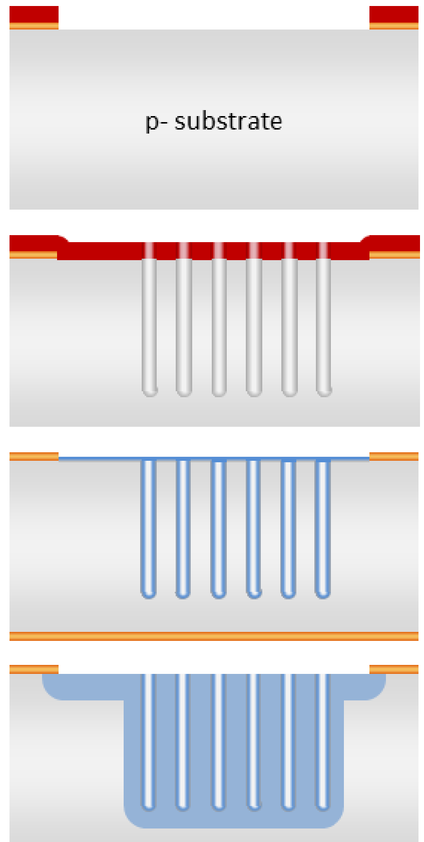
Fraunhofer IISB

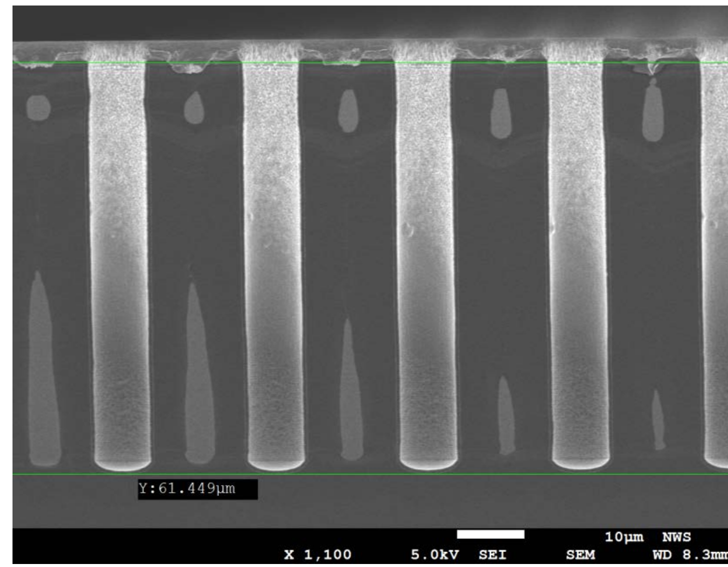
Process flow for fabrication of integrated capacitors

- Trench patterning can be performed with TSV DRIE process (200µm)
  - Implementation of TSV-etching process
    - Diameter: 8µm
    - Spacing: 5µm
    - Depth: 60µm



Hole pattern design



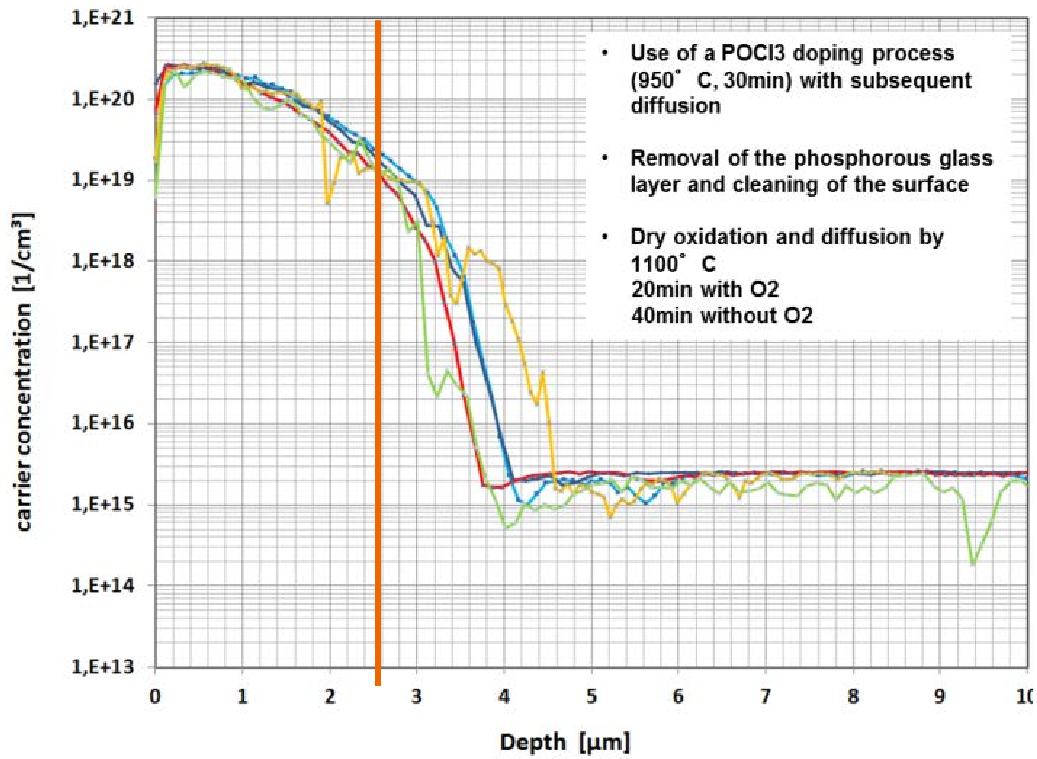


Trench patterns after RIE

Oxidation and phosphor diffusion, removal oxide and back side nitride

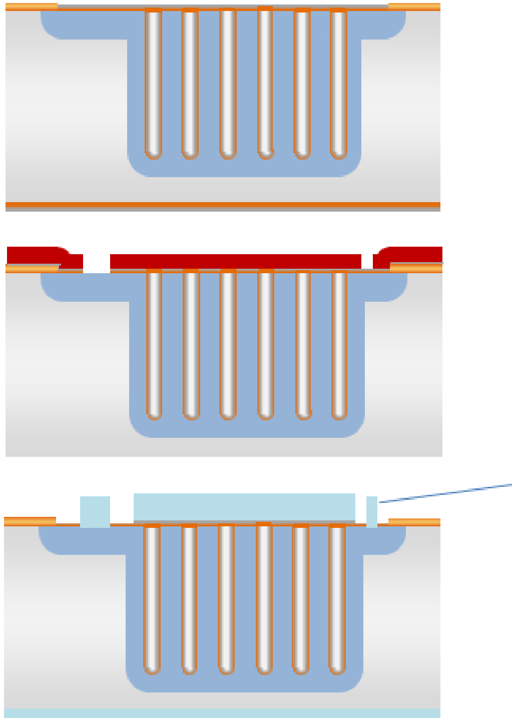
Process flow for fabrication of integrated capacitors

- Process module for junction isolation (n^+-region in p-substrate)
  - Masking of surface with silicon nitride
  - $POCl_3$ doping into trenches
  - Thermal oxidation for diffusion of phosphorous
    - Prevents out-diffusion of phosphorous
    - n^+-region formation in trench region (selective)



Process flow for fabrication of integrated capacitors

- Capacitor stack and metallization
  - Dielectric: 32nm SiO_2 and 52nm Si_3N_4
  - Trench-fill with in-situ doped Polysilicon



Oxidation and deposition dielectric
deposition polysilicon

Lithography 3: Opening substat contact
dry etching polysilicon and dielectric

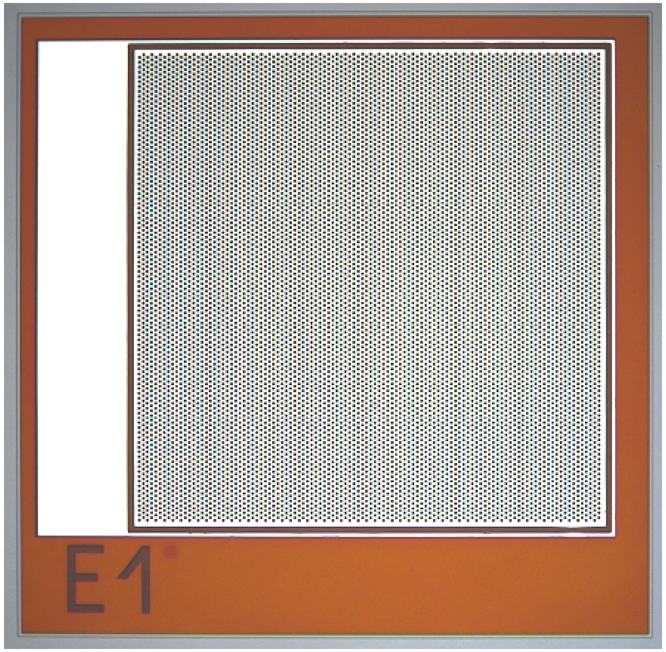
framed substrate contact

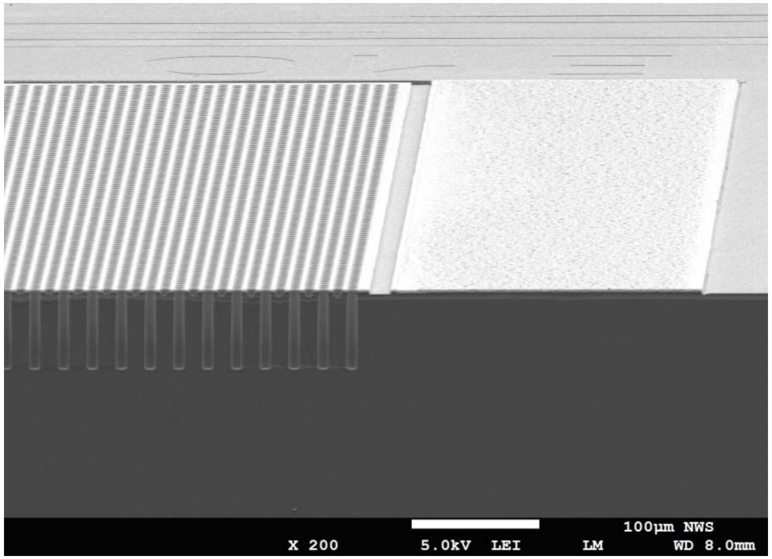
Metal deposition
Lithography 4: dry etching metal layer
Etching Polysilicon with metal mask
Back side metalization

Fraunhofer
IISB

Process flow for fabrication of integrated capacitors

- Optical and SEM images of fabricated devices





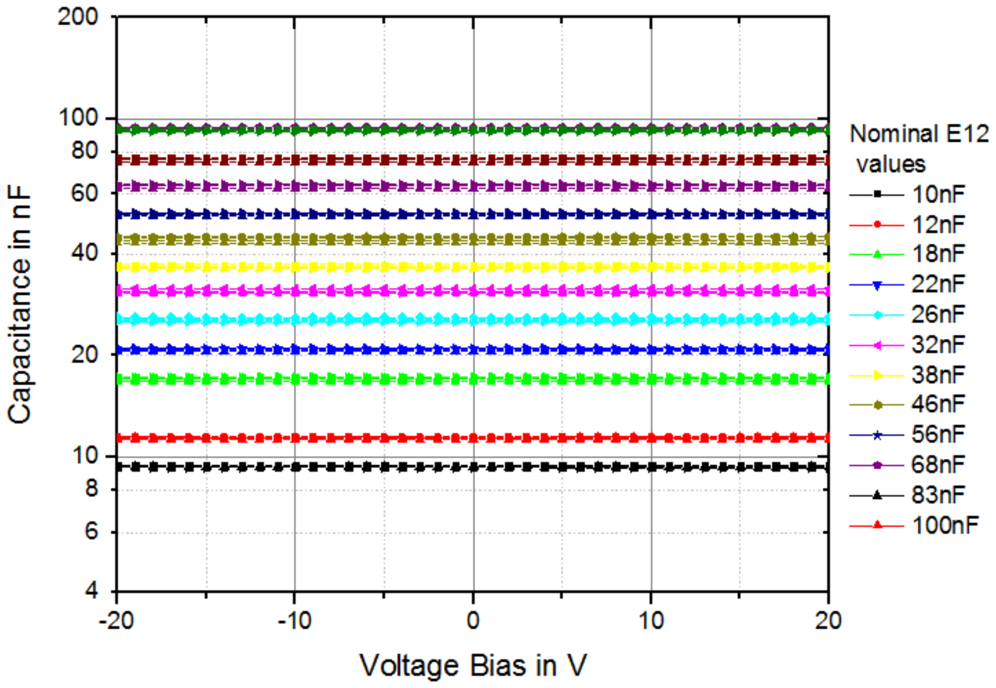
Top-view and cross-section of lateral capacitor with pad

Content

- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

Electrical performance of integrated lateral capacitors

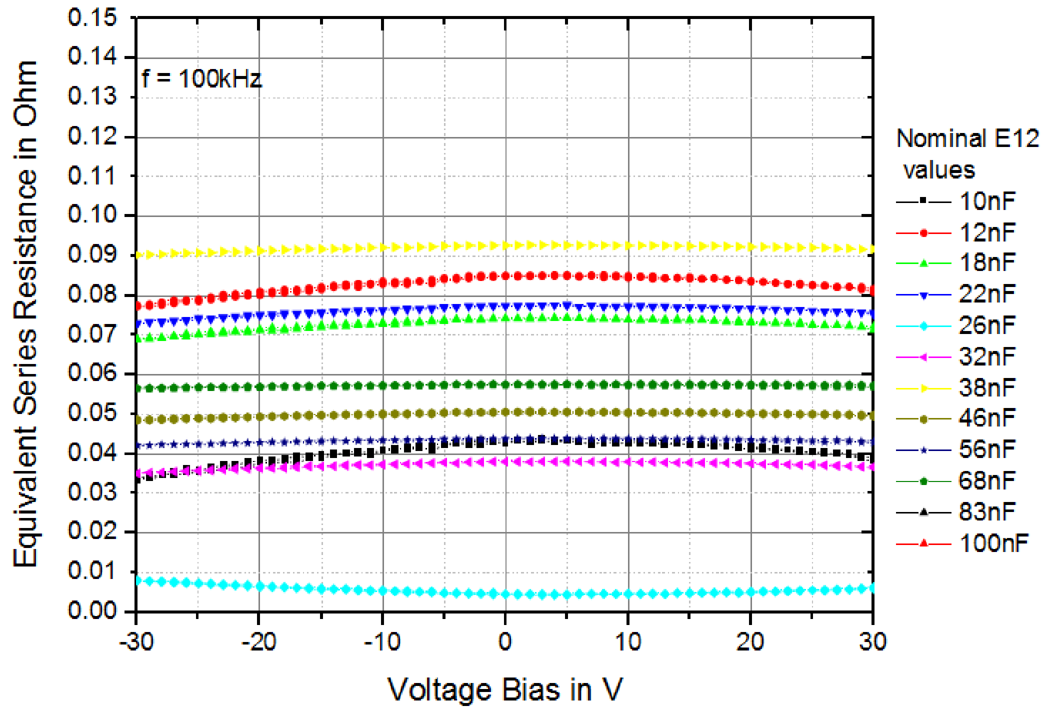
- Capacitance measurements of integrated **E12** series capacitors
  - Voltage-dispersion of capacitance not evident
    due to n⁺-doped trench region (see MOS capacitor theory)
  - Decent E12 series distribution
  - High integration density
    - Area: 1.5 mm² to 15 mm²
    - Capacitance: 9 nF to 90 nF
    - Integration density:
      6 nF/mm²



Fraunhofer IISB

Electrical performance of integrated lateral capacitors

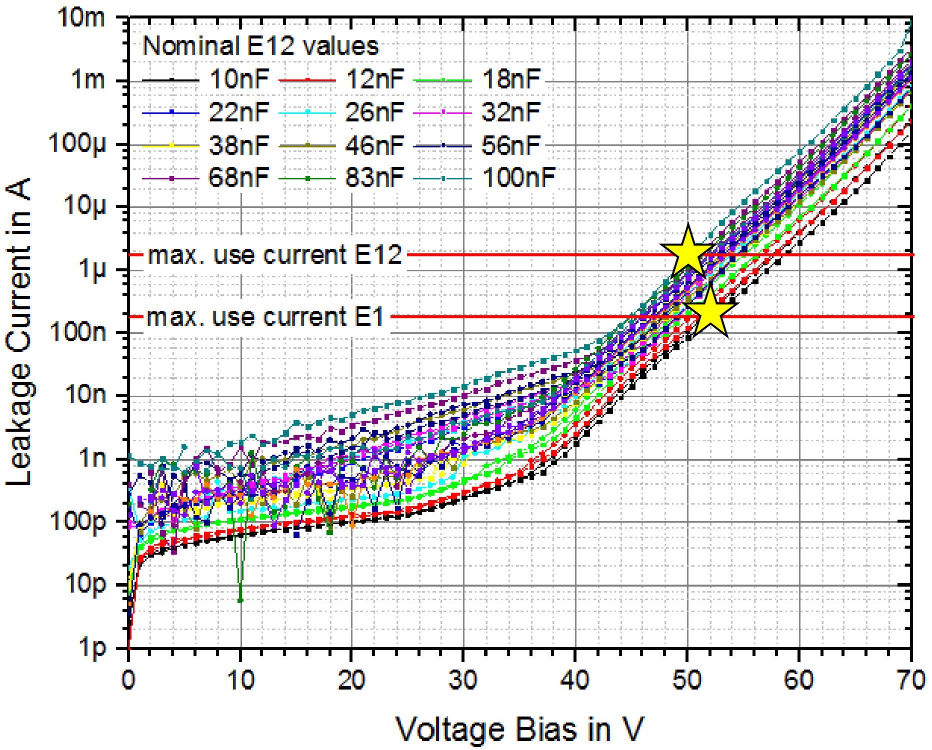
- Series resistance of integrated **E12** series capacitors
  - Low ESR values evident
  - Dissipation factor (tanδ) similar to PEN or ceramic capacitors
  - Measurement at resolution limit (e.g. E5 value)



Fraunhofer
IISB

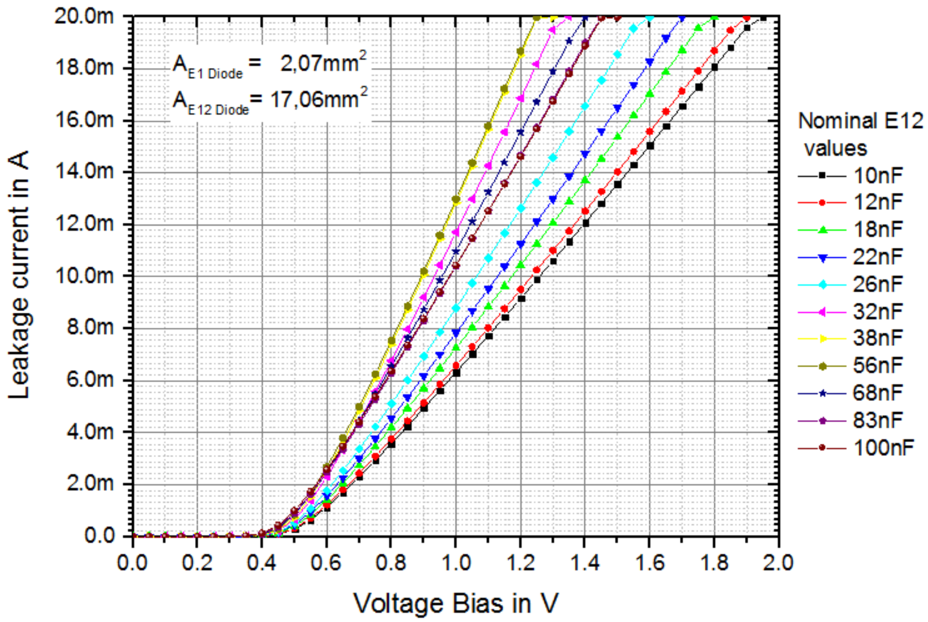
Electrical performance of integrated lateral capacitors

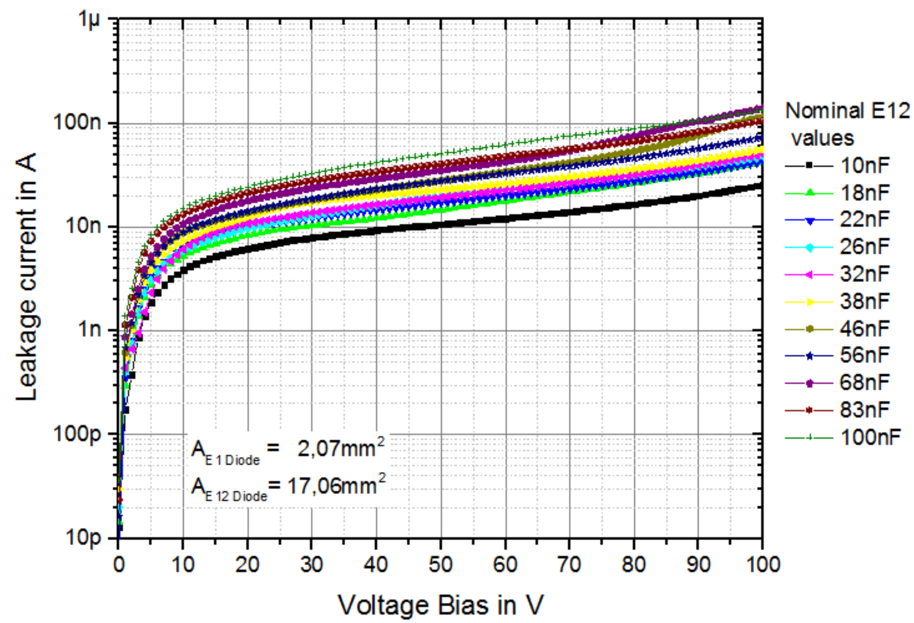
- Leakage current and use voltage of integrated **E12** series capacitors
  - 50V operating voltage can be obtained for all devices
    - Choice of dielectric depends on Mission profile
      - Trade-off: Lifetime vs. integration density
  - Increased leakage current for higher capacitance due to larger device area



Electrical performance of integrated pn-diodes

- Properties of diodes formed though in **E12** series capacitor structures
  - Acceptable leakage current of pn-junctions for isolation of capacitors
  - Blocking voltage exceeds 100V despite lack of junction termination
  - Forward voltage drop exhibits ohmic resistance due to side contacts only





Fraunhofer IISB

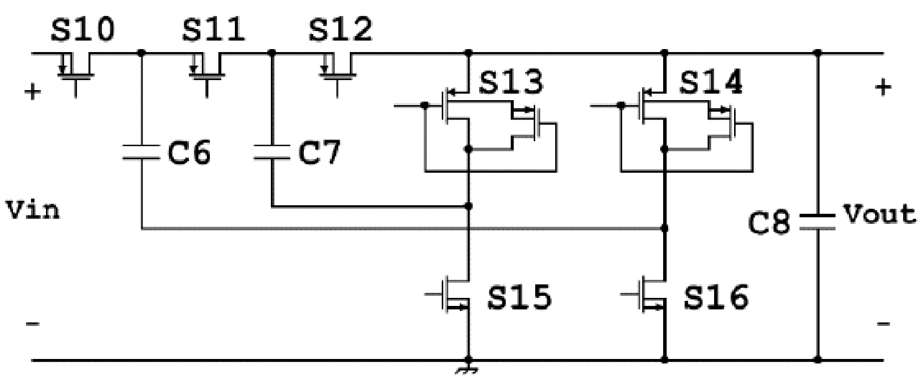
Content

- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

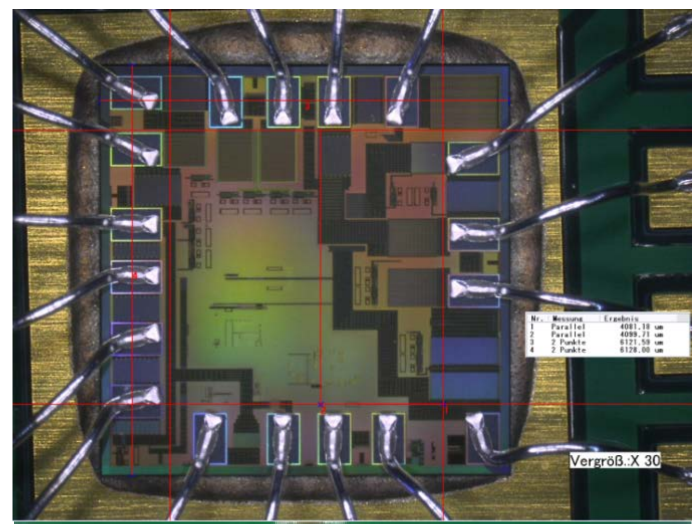
Application example: 48V SMPS with 5V LDO

- Automotive Tested High-voltage and Embedded Non-volatile Integrated SoC platform with 3D Technology
  - Capacitor-based DC/DC converter
  - Power switches are integrated into HV CMOS chip
  - SMD capacitors on PCB

Capacitor based SMPS circuit



Saponara, Ciarpi, IEEE Trans. Circuit & Systems I, 2016

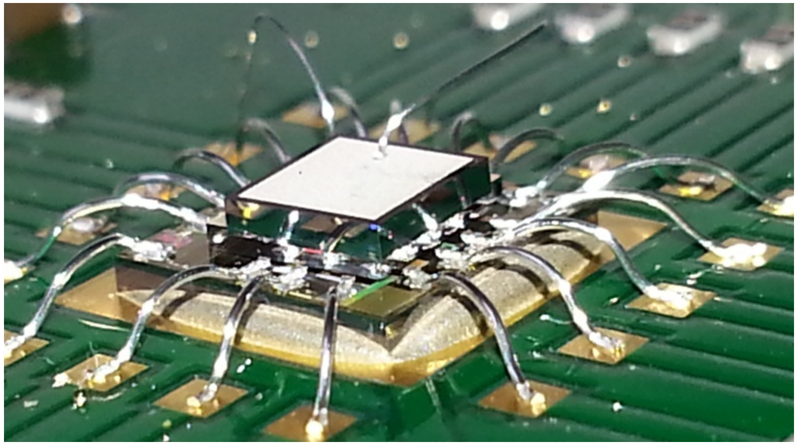


DC/DC converter on PCB

HV CMOS chip

Application example: 48V SMPS with 5V LDO

- Replacement of SMD capacitor on PCB in LDO circuit
  - 200nF SMD capacitor replaced with 50nF integrated capacitor
  - Implementation using an integrated stand-alone capacitor

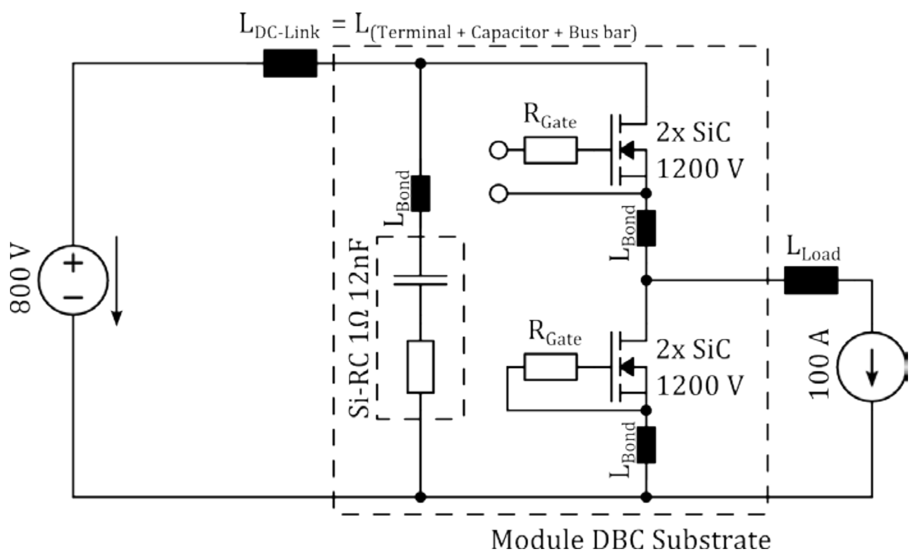


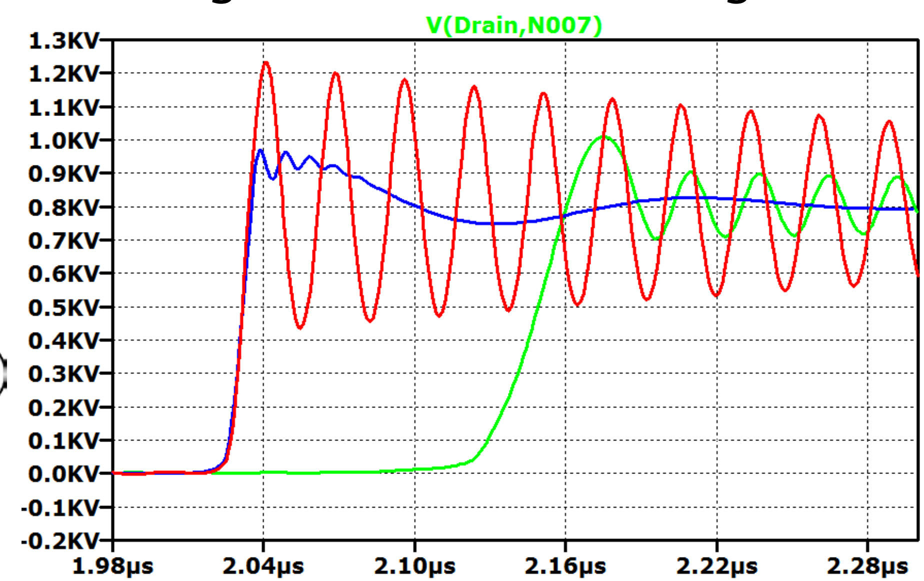
  - Electrical performance of LDO running at 3MHz is similar
    - Voltage ripple
    - Voltage stability under different load currents

→ Benefit of lateral capacitor: It is the interposer!

Application example: Power module w/ 900V RC-snubber

- Enabling conventional power modules for optimum SiC device performance
  - SiC devices are economically feasible under high switching frequencies
  - IGBT-based power modules are not designed for 100kHz+ switching
    - → Parasitic inductances cause over-voltages under fast switching





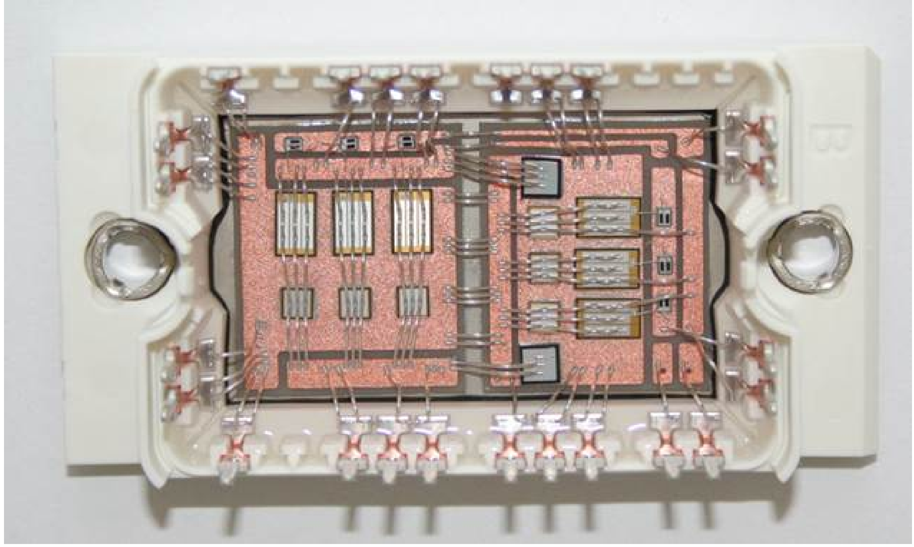
  - Either Low-inductive module design required (additional effort)
  - Or high gate resistance to slow SiC devices down (inefficient)

Application example: Power module w/ 900V RC-snubber

- Enabling conventional power modules for optimum SiC device performance
  - Capacitors with 900V use voltage through scalability of manufacturing technology

    → Thicker dielectrics are used
  - Conventional EconoPak (Danfoss) was retrofitted
    - 6x 1200V, 25A SiC VDMOS (Cree)
    - 2x Si RC-Snubber

    → 116A possible due to reduced switching losses at 130kHz
  - Without RC-Snubber 8 SiC-FETs are necessary



Content

- Motivation: 3D integration of power electronics
- Experimental: Process flow for integration of passive networks
- Results and Discussion
  - Electrical properties of integrated capacitors
  - Electrical properties of integrated diodes
- Application examples
  - Integrated 48V DC-DC converter
  - 900V Full-SiC converters with conventional (IGBT-type) power modules
- Conclusion

Conclusion

- Integration of lateral capacitors on Si interposer possible
  - Conventional CMOS processing technology and equipment
  - For 50V application 6 nF/mm^2 and low ESR achieved
  - Devices are electrically isolated through pn-junctions

- Applications benefit from on-chip capacitors
  - Higher switching frequencies can be used
    - 48V DC-DC converter with capacitive energy transfer feasible
    - Retrofitting of conventional power modules with SiC MOSFETs up to 900V DC link voltage possible
      - Reduced switching losses → Less SiC chip area required

- Based on platform technology for automotive-grade HV-CMOS with TSV

Thank you for Your attention!

Acknowledgements

The research leading to these results has received funding from the European Community's Seventh Framework Program FP7 under grant agreement no. 619246 (ATHENIS_3D).