

# Integration of Multi-level MOEMS Structures on CMOS for Spatial Light Modulators

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**Abstract** — A new generation of spatial light modulators (SLM) was developed based on SiO<sub>2</sub> sacrificial layer technology and multi-level actuator designs. In this paper, we will present the current status of monolithic integration of MOEMS structures on CMOS backplanes, advantages of the SiO<sub>2</sub> sacrificial layer process and of a new structural MEMS material used to achieve long-term stable operation of high reflective mirrors.

This sophisticated micromachining technology will be demonstrated presenting actual spatial light modulator developments and key parameters of these devices.

## 1 Introduction

Spatial light modulators (SLM) as a kind of optical MEMS (micro opto electro mechanical systems also called MOEMS) are based on arrays of individually deflectable micro-mirrors. Depending on their field of application the mirror deflection can be realized as torsional, piston or a combination of both. Such spatial light modulators are for example used as high speed pattern generators in DUV lithography, for mask inspection, for wave front correction in adaptive optics and for projection systems.

Especially, an analogue deflection scheme is often essential for many applications. Therefore a drift free mirror deflection and a superior mirror planarity are major challenges for these optical MEMS devices. Using a CMOS compatible surface micromachining process micro-mirror arrays are fabricated on customized CMOS backplanes with various mirror sizes. Current research shows that mirrors with pitches as low as 8µm can be fabricated using the IPMS multi-level MOEMS technology.

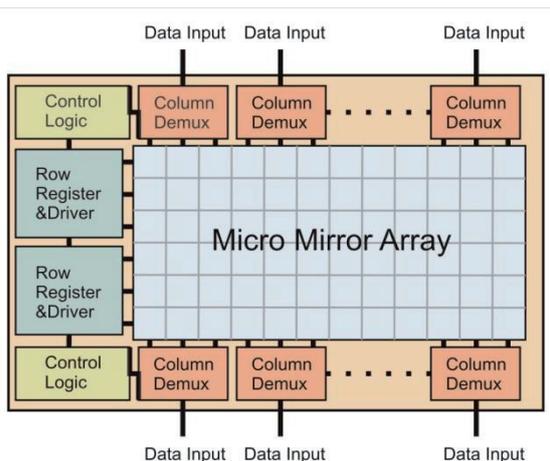


Fig.1: Schematic drawing of a SLM chip

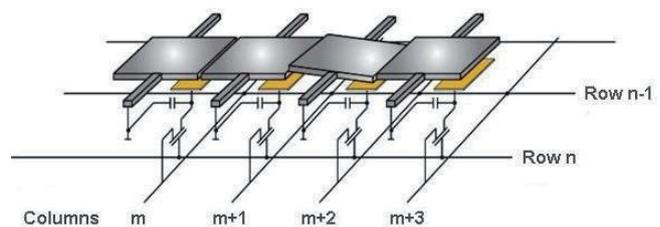


Fig.2: Schematic of micro-mirrors with underlying DRAM like circuit

Spatial light modulators (SLM) may contain up to millions of matrix addressed mirrors that can be individually deflected. Figure 1 shows a basic schematic of such a SLM device. The high level of integration that is needed to manufacture these devices is achieved by the monolithic integration of MOEMS with a high voltage CMOS backplane. To supply every single mirror with one or more individual voltages the mirror array is driven by a circuit, which is similar to a DRAM, capable of storing analogue voltages. The micro-mirrors translate the analogue voltages that are stored in simple DRAM cells underneath the mirrors, as depicted in Figure 2, into an analogue deflection state. The deflection principle is based on the electrical attraction forces between two plates of an air-gap capacitor where one movable plate is supported by a micro patterned spring structure to provide a restoring force.

## 2 Basic Actuation Principle

As a simple example the deflection characteristics of a linear suspended piston-type MEMS drive will be derived. The corresponding simplified schematic is shown in Figure 3.

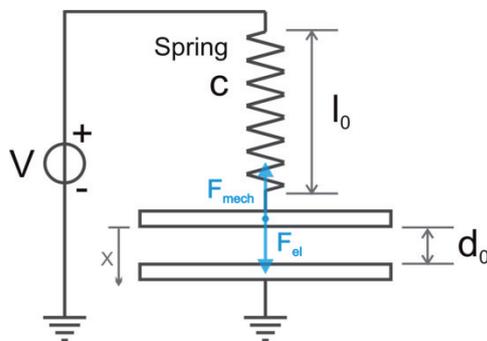


Fig.3: Simplified schematic of a piston actuator

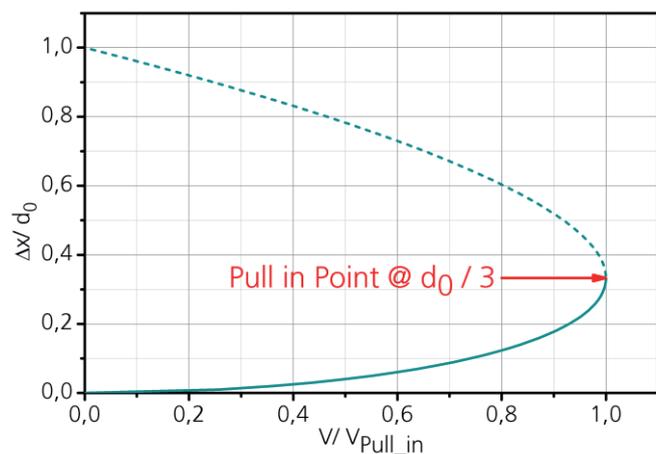


Fig.4: normalized deflection characteristics of a piston actuator

The force that is generated by the electric field inside the air-gap is given by equation (1) where  $A$  is the capacitor area,  $d$  the distance between the two plates and  $V$  the applied voltage respectively.

$$F_{el} = \frac{1}{2} \epsilon_0 A \left( \frac{V}{d} \right)^2 \text{ with } d = d_0 - \Delta x \quad (1)$$

One of the capacitor's plates is movable and suspended by a spring. This spring provides a restoring force if the plate is displaced by  $\Delta x$  from its zero position, given at the capacitor plate distance  $d_0$ . This mechanical force is given by equation (2) where  $c$  is the spring constant.

$$F_{mech} = -c \Delta x \quad (2)$$

If equation (1) and (2) are combined and solved for the driving voltage  $V$ , deflection characteristic is given by equation (3).

$$V = \sqrt{\frac{2c\Delta x}{\epsilon_0 A}} (d_0 - \Delta x) \quad (3)$$

Looking at the normalized deflection characteristics for a piston type mirror with a linear spring plotted in Figure 4, it can be seen that the equilibrium of electrical and mechanical force becomes unstable if the plate is moved by more than 1/3 of the zero position plate distance  $d_0$ . This is the so called pull-in point that is caused by the strong nonlinearity of the electrostatic force in dependency of the plate distance  $d$  given by equation (1). Once this point is exceeded the electrostatic force grows faster than the mechanical restoring force of the spring resulting in an immediate touchdown of the movable plate.

For analogue operations, micro-mirrors need to be operated well below the pull in point in order to avoid any unwanted pull down. Therefore the air-gap for a piston-type actuator with a linear spring must be at least 3 times higher than the expected stroke.

Other types of deflections like torsion or a combined torsion and piston movement can be achieved by an appropriate spring and driving electrode design. For a pure piston-type actuation the driving electric field inside the air-gap must be uniformly distributed and the springs must be located in a manner to suppress any kind of torsion. If torsional actuation is needed the actuator needs to be suspended by springs that allow torsional movement. To create the necessary torque the driving electrode is located asymmetrically with respect to the torsional axis. Figure 5 compares the basic schematics of a piston and a torsion actuator.

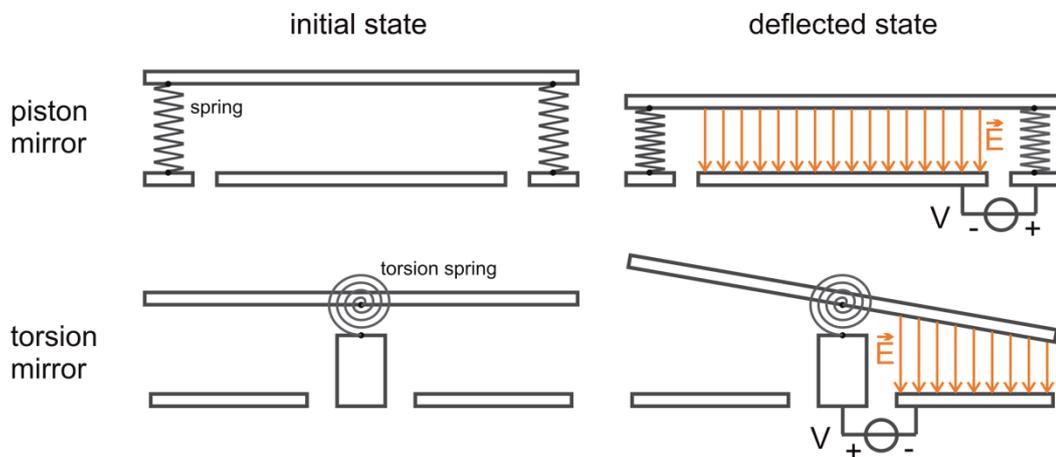


Fig.5: Schematic drawing of piston and torsion MEMS actuators

### 3 Multi-level MOEMS Process

One key element of the successful integration of MOEMS structures on CMOS backplanes is the sacrificial layer process. These sacrificial layers define the air-

gaps necessary for the movement of the MEMS structures and it fixes all fragile MOEMS structures, i.e. springs, stoppers and mirrors throughout the wafer processing. As one of the last process steps the sacrificial layers are removed by an isotropic etch in order to create a free movable structure.

The IPMS MOEMS process uses PECVD  $\text{SiO}_2$  as sacrificial layer material that is finally removed by a gas phase hydrogen fluoride etch<sup>1</sup>. The advantage of using  $\text{SiO}_2$  is that standard CMP processes from back end of line (BEOL), with low defect levels and excellent planarization results, can be used to smooth out the sacrificial layers. It is essential for micro-mirror arrays to include several CMP steps throughout the CMOS and MOEMS processing to maintain the high surface quality, especially surface planarity needed for optical systems. A minor drawback of  $\text{SiO}_2$  sacrificial layers is the need for a separate etch barrier to protect the underlying  $\text{SiO}_2$  based ILDs of the CMOS backplane during the release etch. Since the etch barrier layer needs to be a dielectric, which is chemically inert to the hydrogen fluoride gas phase etch,  $\text{Al}_2\text{O}_3$  was chosen over a few other materials<sup>2,3</sup>.

The second important component for such MOEMS structures is the choice of materials to create structural elements. As different MEMS layers serve different purposes the materials must be chosen with respect to their function (Young's modulus, creep, and reflectivity) to ensure a stable and outstanding MEMS performance.

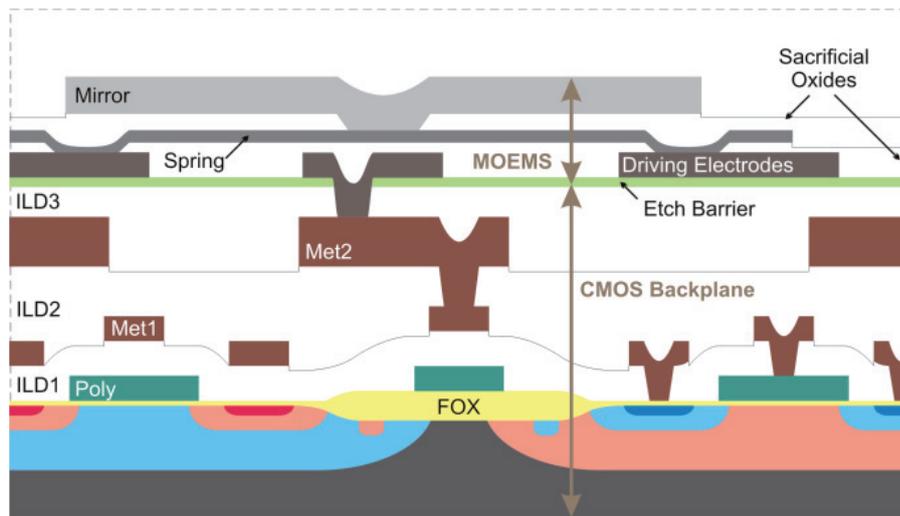


Fig.6: Two-level MOEMS structure

Therefore a multi-level MOEMS process is used where each level represents a different function by using an appropriate material. Depending on the maximum desired deflection a two/three-level MOEMS process can be selected. For rather small deflections a two-level MOEMS structure, consisting of mirror layer and spring layer (as shown in cross section in Figure 6), will be sufficient.

According to the pull in criterion a larger deflection requires a bigger air-gap. This will lead to a reduced electrostatic force since it is proportional to  $1/d^2$  as stated in equation (1). Increasing the driving voltage is not an option since it is limited by the CMOS backplane. Therefore the spring must be made softer to compensate the

weaker electrostatic force and to allow a higher deflection. Micro-mirror structures with very soft hinges for large deflections are fabricated with a three-level MOEMS Process<sup>8</sup>. Figure 7 shows a cross section of such a three-level MOEMS structure including the underlying CMOS backplane. In order to strengthen the support structures of the thin spring layer a third so called reinforcement layer was integrated into the micro-mirror structure.

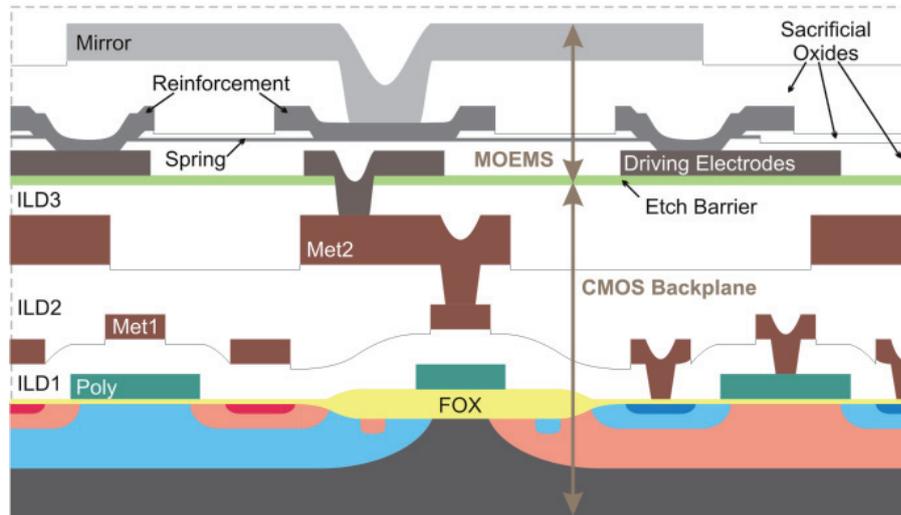


Fig.7: Three-level MOEMS structure

The following two pictures compare the deflection characteristics of 16µm x 16µm micro-mirrors fabricated by the two-level and the three-level MOEMS process. Figure 8 shows the average deflection characteristic of two-level torsional micro-mirror with a total air-gap of 0.8µm, and Figure 9 shows the average deflection characteristic of a three-level torsional micro-mirror with a total air-gap of 1.8µm respectively. Torsional micro-mirrors with a 16µm pixel pitch reach deflections up to 450nm if fabricated using the three-level MOEMS process.

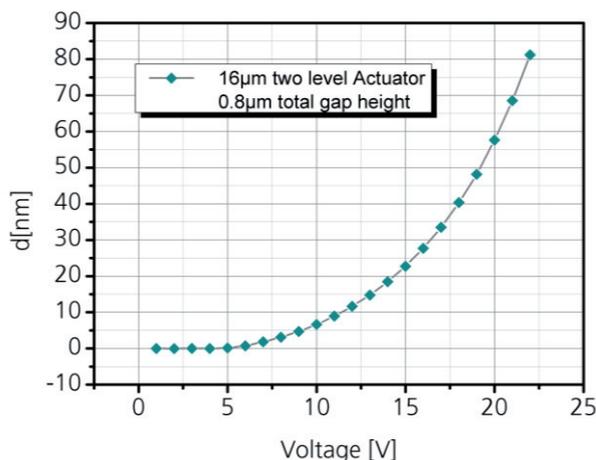


Fig.:8 deflection characteristics two-level 16 x 16µm<sup>2</sup> torsional mirror

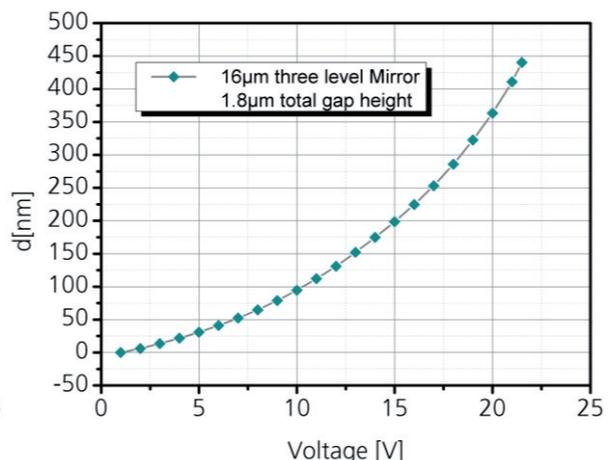


Fig.9: deflection characteristics three-level 16 x 16µm<sup>2</sup> torsional mirror

For a precise analogue operation the spring layer needs to be perfectly elastic to avoid instabilities caused by material creep. Therefore an amorphous TiAl alloy is used as spring material<sup>4</sup>. The example depicted in Figure 10 shows a two-level tilt mirror with a TiAl spring that has been continuously deflected for 30min by approx. 80nm. The TiAl springs are considered to be drift free because the measured drift lies well below the measurement accuracy.

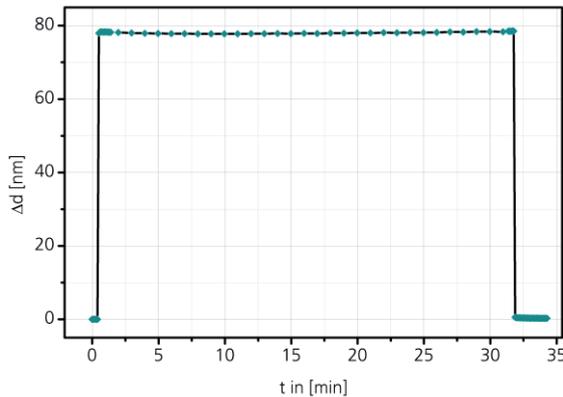


Fig.10: Long term static deflection of a tilt micro-mirror

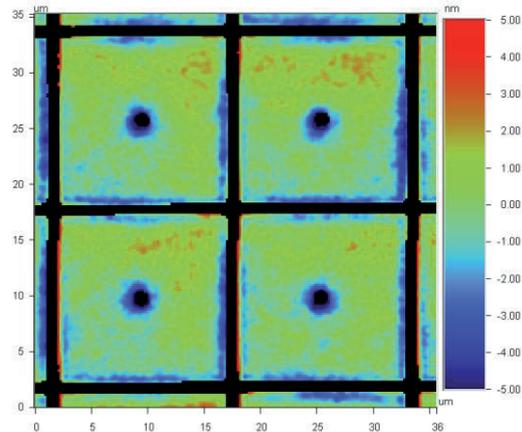


Fig.11: WLI height profile of 4 micro-mirrors

This multi-level setup allows the usage of an adapted material as mirror layer. Aluminium based alloys are CMOS compatible, providing good planarity and high reflectivity over a wide wavelength range. For applications where higher reflectivity is necessary dielectric layers can be used in addition<sup>5</sup>. A white light interferometer height profile of 4 mirrors (pixel pitch is 16 $\mu$ m) based on aluminium alloys is shown in Figure 11 and shows a superior planarity in the nm range.

## 4 Application examples

### 4.1 1 Megapixel SLM

One application of micro-mirror arrays is the use as pattern generator in DUV excimer laser based micro lithography systems like mask writers<sup>6</sup>. The 1 Megapixel SLM depicted in Figure 12 contains 2048 x 512 individually deflectable tilt mirrors. Such a high count of mirrors is needed to maximize the throughput. The 1 Megapixel SLM has an image frame rate of 2kHz resulting in a writing speed of 2 GPixels/s with true grey levels in real time. The imaging principle is based on Fourier optics and spatial filtering. It enables a sub-grid addressing by the true grey scaling feature of these analogue SLM devices<sup>7</sup>. The operation wavelength is 248nm. Undelected mirrors will result in white pixels and black pixels are created if the mirrors are tilted by 62nm. The micro-mirrors of the 1 Megapixel SLM have a pitch of 16 $\mu$ m x 16 $\mu$ m.

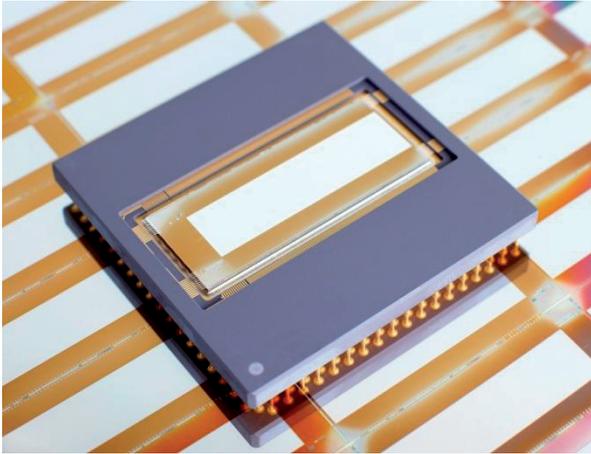


Fig.12: 1 Megapixel SLM chip

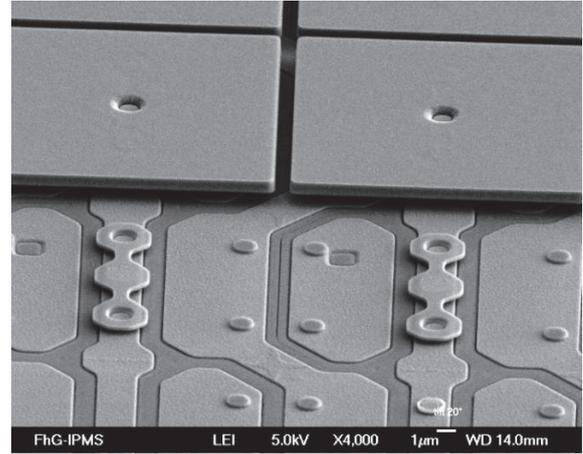


Fig.13: SEM image of micro-mirrors on the 1MPixel SLM

Figure 13 shows a SEM image of the two-level tilt mirrors consisting of an Al based mirror plate and torsional TiAl springs that are hidden underneath the mirror (mirrors are removed in lower part of this picture).

#### 4.2 64k Pixel MMA

A more versatile SLM device capable of operating at wavelengths from 240-800nm is shown in Figure 14. The operation at higher wavelengths requires a larger deflection of its tilt mirrors to achieve reasonable contrast values<sup>8</sup>. The SLM chip has an image frame rate of 1kHz and contains 256 x 256 individually deflectable mirrors with a pitch of 16µm x 16µm.

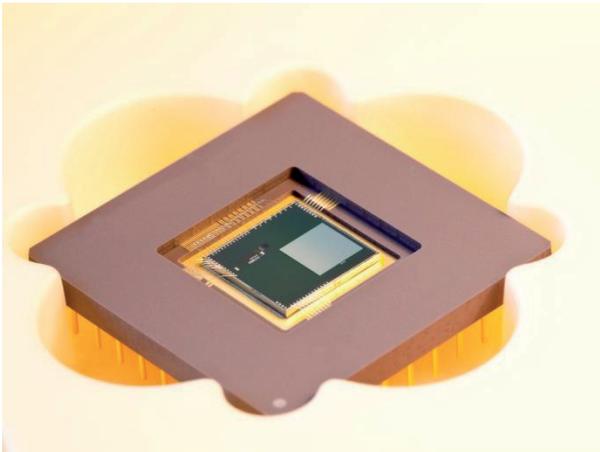


Fig.14: 64k Pixel MMA Chip

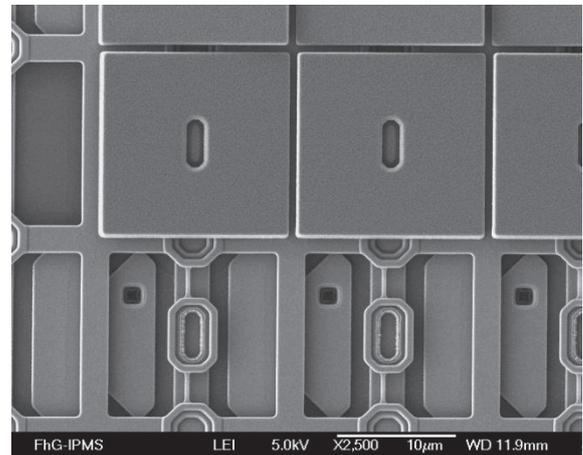


Fig.15: Mirror and hinge structure in of a 64k Pixel SLM chip

This device is fabricated using a three-level MOEMS process<sup>8</sup> with an additional reinforcement layer. The SEM image in Figure 15 is showing the structure of a three-level micro-mirror. Compared to a typical two-level actuator an additional hinge reinforcement layer is essential to anchor the entire structure (i.e. posts) due to very thin hinge layers (down to 70nm).

## 5 Conclusions

A new process of monolithic integration of MOEMS structures using micromachining was successfully developed. One feature of this micromachining process is the SiO<sub>2</sub> sacrificial layer technology to achieve defect free oxide layers with sophisticated surface planarity using standard CMP processes. Through a separation of hinge and mirror levels, and in this sense also the material, it is now possible to optimize layers properties independently. The overall thermal budget of the IPMS MOEMS process on CMOS backplanes stays well below 440°C to avoid any damage of the CMOS interconnections. A three-level actuator design allows a complete tuning of deflection characteristics which leads to new applications for SLM devices.

## 6 Acknowledgment

The author would like to thank all IPMS Colleagues who have contributed to the development of the multi-level MOEMS technology with careful and accurate work e.g. in process module development, wafer processing, simulation and device characterisation.

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