Advanced Wet-Etch-Only Process for Complete Tri-Layer Rework

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A tri-layer patterning technique is used for high numerical aperture immersion lithography at 28 nm node. The tri-layer consists of a photoresist (PR) deposited on a silicon-containing anti-reflective coating (SiARC) above an organic planarization layer (OPL). Defective PR processes (e.g. overlay, over-exposure, residues) are repeatedly being reworked in high volume manufacturing. Due to the different chemical composition of the three layers, multiple etch processes are necessary. In this work, we investigate a wet-etch-only tri-layer rework approach that has the advantage of lower material damage, cost reduction and increased throughput. Complete stack removal and low defect levels on patterned 300 mm wafers could be achieved.

Introduction

Downscaling of integrated circuits has required high numerical aperture immersion lithography and tri-layer lithography stack since the 45 nm technology node [1]. The tri-layer lithography stack consists of an organic planarization layer (OPL) or spin-on carbon (SOC), a silicon anti-reflective coating (SiARC) and a photoresist (PR) as illustrated in Figure 1. The OPL is typically an organic layer that will provide adequate etch resistance and planarity during etching into low-k and ultra-low-k (ULK) dielectrics. The SiARC will ensure an improved etch selectivity to thinner PR as well as enhance the reflectivity control [1] [2] [3].

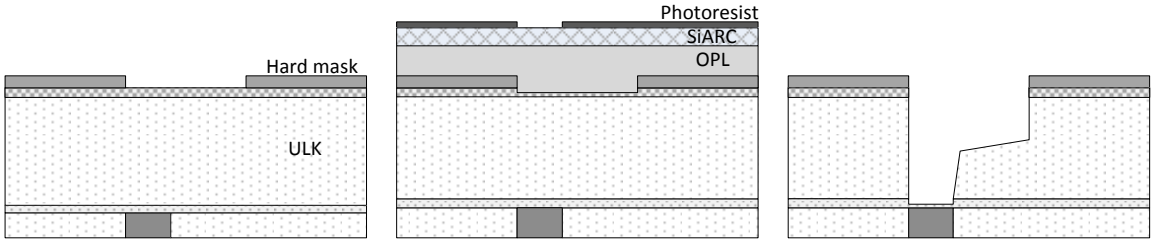

Figure 1. Trench-first-metal-hard-mask dual damascene integration flow with deposited ULK + MHM (left), OPL/SiARC/PR tri-layer stack (middle) and etched structures (right).

Patterned PR layer critical dimensions (CD) loss, overlay, over-etching and residues are common defects during semiconductor manufacturing. To avoid damage transfer and consequent yield loss, multiple lithography rework cycles are usually introduced. The complexity of the tri-layer stack makes the rework process very challenging. There are several approaches for reworking the tri-layer stack. They can be classified into selective and complete rework.

Selective rework implies the removal of PR selectively compared to the SiARC. The advantage is that it is a one process rework and has a low chemical consumption. The selective rework approach could be dry, but it has several disadvantages like remaining residues, SiARC thickness loss and optical properties shift [4]. Therefore, this process is usually a solvent based wet process (e.g. PGMEA). Even though these aforementioned disadvantages can be avoided, there may be resist pattern footing and high defect counts [1]. Therefore, it is advisable to remove the complete tri-layer and reprocess it.

The complete rework is usually performed with several processes. The common rework for Back-End-of-Line (BEoL) interconnects 28 nm technology node structures is a dry-wet-dry-wet process (Figure 2, left). The first step is a resist ash with simultaneous SiARC oxidation. The SiARC film requires high Si content for acting as reliable mask, thus is hard to be removed by dry etch [1]. As a consequence, a wet-etch process is executed, followed by an OPL plasma strip. Finally, a water rinse is done to remove the remaining residues. Even though this rework results in low defect levels, it has several disadvantages. Firstly, the resist ash and the OPL plasma strip cause damage to the dielectric layer, since these two processes are usually executed with oxygen. Although the dielectric cap protects the ULK, oxygen radicals can reach depths of several nanometers, damaging the ULK and consequently increasing its k value [5]. Secondly, the ion bombardment from plasma causes TiN hard mask damage (e.g. CD loss, roughness, lower thickness, and TiN oxidation issue). Additionally, four multiple processes (i.e. a dry-wet-dry-wet process) are required in order to remove the complete tri-layer stack, which decreases throughput.

The 28 nm technology node is a ‘sweet spot’ in terms of costs per die without the need to introduce new expensive lithography processes. Tri-layer lithography stack rework is required to avoid yield loss but it causes low throughput, since several intermediate processes are necessary. Therefore, the industry is trying to find a complete rework that can be executed in just one process, reducing the overall cost by increasing throughput. A complete rework with dry processes has been reported by Mattson et al. [6]. However, it has difficulties in the dry etch of SiARC when the silicon content is high. Furthermore, it is actually a two-step process rework (dry-wet) since a wet clean process is required at the end. Additionally, the aforementioned plasma induced damage from dry etch cannot be avoided. The complete rework with wet processes has been further explored. The commonly used chemicals contain sulfuric acid and hydrogen peroxide mixtures. However, long process times and temperatures higher than 60 °C were needed [2]. It has been shown that SiARC with an ultra-high silicon content of 42 % could not be removed with Piranha [7]. Moreover, the compatibility with TEOS cap and TiN damage was not examined.

This work evaluates a complete wet etch tri-layer rework approach which removes SiARC with high silicon content, increases the throughput and does not damage the underlying titanium nitride hard mask, dielectric cap and ultra-low-k material. Our process approach is illustrated in Figure 2.

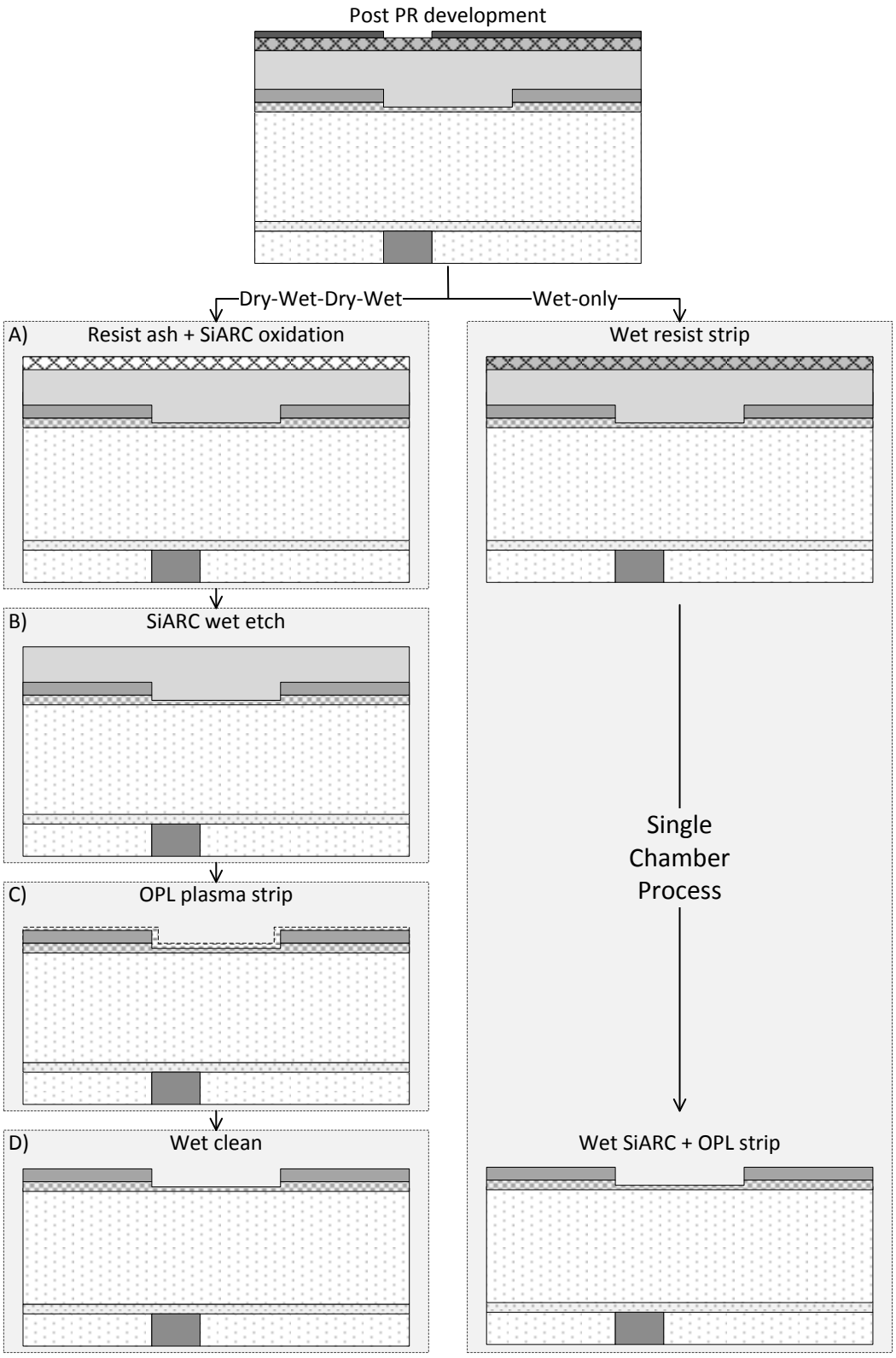

Figure 2. Comparison between dry-wet-dry-wet (left) and advanced wet-only (right) tri-layer rework process for 28 nm dual damascene integration. Common process consists of A) O_2 plasma PR ash with simultaneous SiARC oxidation B) Wet etch of semi-oxidized SiARC C) Dry etched OPL and D) Wet cleaning of residues. In contrast, the wet-etch-only approach consists of a single-process containing two steps.

Methodology

Our current tri-layer rework evaluation investigated 14 chemicals from 6 different suppliers screened on 5 thin film materials (PR, SiARC, OPL, TiN and TEOS), deposited on 300 mm wafers. In order to reduce the number of experiments on blankets and on patterned wafers, an experimental workflow was elaborated.

The first experiments were carried out on samples in a beaker for identifying the most promising chemicals. The samples were obtained from breaking the wafers into pieces, to determine chemicals' ability to strip the PR, SiARC and/or OPL without damaging the TiN and TEOS underneath. Care was taken for the thermal budget to guarantee the stability of the chemicals. All experiments in beaker were processed at 50 °C with controlled stirring for 2 minutes. Reflectance amplitude, phase shift and thickness were measured on samples by spectroscopic ellipsometry on a Semilab SOPRA EP5 Tool. Later, the experiments were executed on 300 mm wafers industry standard equipment. The wet-strip was performed on a SEMITOOL Raider SP capsule. Thickness was measured by spectroscopic ellipsometry on a FX100 KLA Tencor. Roughness was obtained by confocal microscopy with µSurf Mobile from NanoFocus. Finally, tests were performed on patterned wafers. 28 nm technology node structures on 300 mm wafers are prepared by an external foundry partner. The defect scans and SEM pictures were done there as well. Therefore the processed wafers were sent back with controlled queue times and tight logistics.

Results and Discussion

Almost all tested chemicals were able to strip the PR and OPL easily. Consequently, we chose the chemical (hereinafter A), which requires the least time to strip the PR. The challenging silicon-rich SiARC layer was only strippable with one chemical (hereinafter B). Unfortunately, this chemical is not able to strip the PR in a suitable amount of time. The ability of B to remove the SiARC was determined with ellipsometry. The impact of B to TiN was verified by comparing the square roughness (Sq) of a pristine and a treated sample. With Sq of 3.5 nm before and 3.7 nm after the treatment, non-damage might be assumed. Figure 3 shows the plane and 3D roughness map of both.

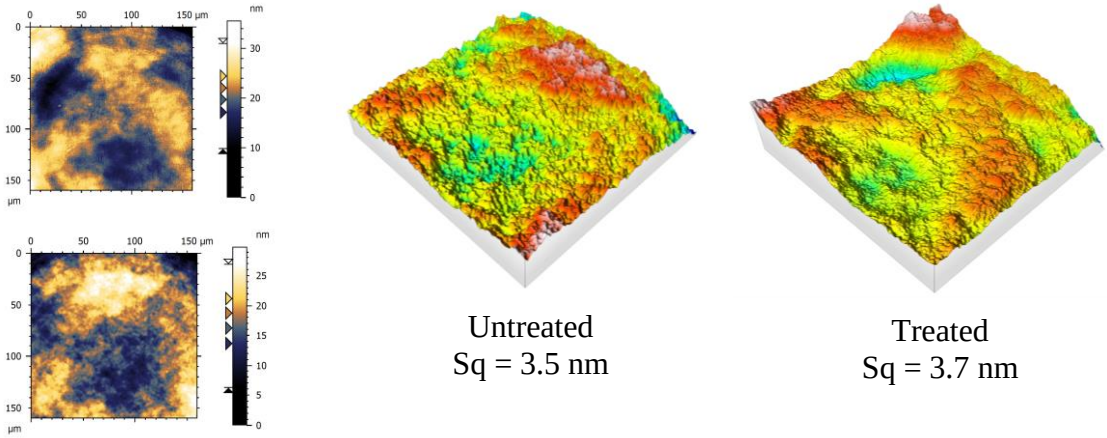

Figure 3. Plane and 3D square roughness map of an untreated (top left) and treated (bottom left) TiN film measured with confocal microscope.

Because PR and SiARC couldn´t be removed successively with one solvent, the necessity of a multistep wet process was obvious. Precisely, a sequence of two steps was determined, at which the first one removes the PR and the second one the SiARC and OPL. This sequence was successfully applied on a 28 nm patterned wafer and is shown in Figure 4.

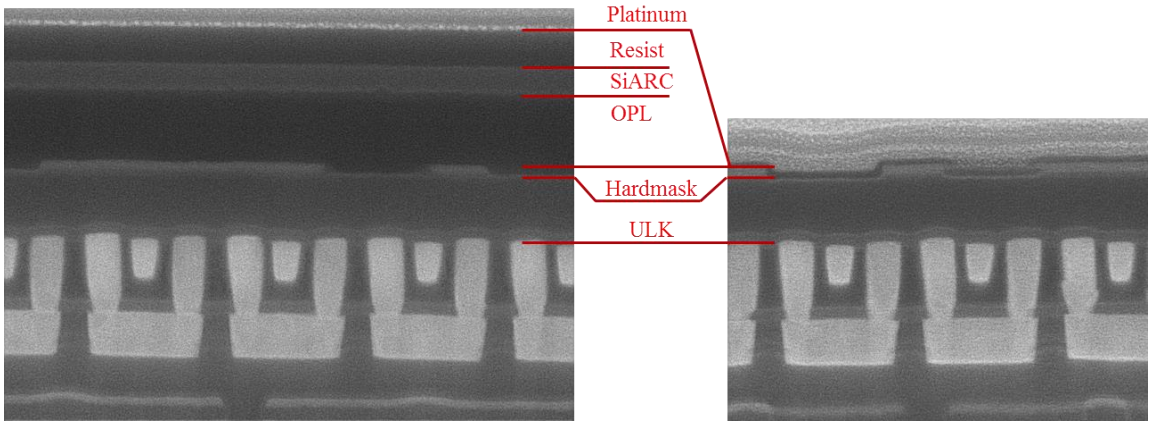

Figure 4. Cross section SEM with FIB of pristine sample with complete tri-layer stack (left) and successful reworked (right).

Initially, the recommended water rinse after the tri-layer wet-strip led to an unexpected high defect level. A SEM top view identified these defects as drying marks, due to an insufficient rinse. By replacing the water by isopropanol these drying marks could be avoided and the defect level reduces remarkably as illustrated by Figure 5.

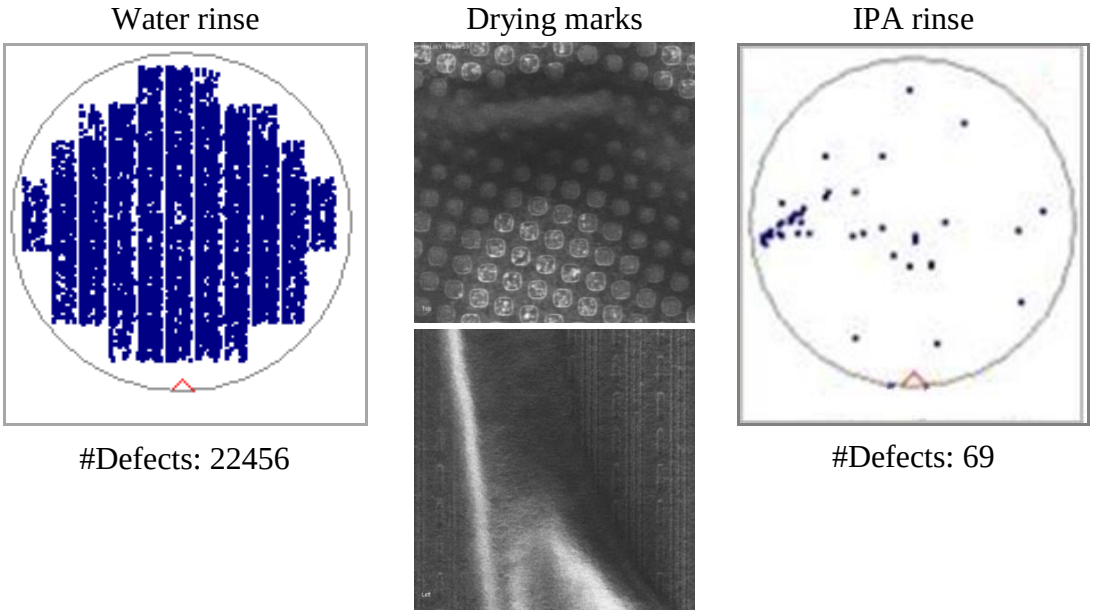

Figure 5. Defect scans of reworked tri-layer with insufficient water rinse (left) and successful IPA rinse (right). Top view SEM pictures of water rinsed sample with drying marks (middle).

Conclusion

In this work we investigated a complete wet-etch-only tri-layer rework approach. We found a possibility by using two chemicals successively, which is able to wet rework the tri-layer stack, without damaging the underlying material. Replacing the water by isopropanol as final rinse process offers a solution to achieve the required drying performance and reducing the number of defects. Most notably, our complete tri-layer rework increases throughput and lowers the overall cost, due to less intermediate processes. This work is opening opportunities to make the tri-layer rework even more profitable.

Acknowledgments

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