A Multibit Continuous-Time Delta-Sigma ADC for Direct Conversion of CdZnTe Detector Arrays

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Abstract

Beside the traditional signal processing channel for radiation detector arrays based on multiple analog filter stages, a new direct analogue to digital conversion strategy is presented in this paper. The main building block of the new channel topology is a continuous-time analog to digital converter. This paper presents the design and implementation of a 78 dB SNR multibit continuous-time delta-sigma ADC. Such ADC is dedicated to the readout of CdZnTe detector arrays at the bandwidth of 625 kHz. This ADC offers the possibility to move most signal processing steps like pulse shaping, energy detection and timing analysis into the digital domain. The die area and power consumption can be reduced by using digital filtering and advanced signal processing algorithmen. The delta-sigma ADC has been designed in an 180nm 1P6M CMOS technology. The circuit consumes 3.8 mW from 1.8 Volt supply.

I. System description

Large-area gamma-ray detection is a base technology for different imaging methods in medical applications. Single photon emission computed tomography (SPECT) and positron emission tomography (PET) are only two examples. The development of sensors for these applications is an ongoing process. Cadmium zinc telluride (CdZnTe) detectors are promising candidates for room temperature operated radiation detection sensor arrays. Beside the sensor itself the signal processing strategies have to be improved and optimized for multi-channel applications. Signal processing for nuclear imaging applications has been developed over several decades [1]. The use of large detector arrays in combination with integrated signal processing offers the possibility to transfer new signal acquisition and processing concepts from other fields. During recent years many traditional analog processing concepts have been replaced by direct analog to digital conversion in combination with digital signal processing. The main reason for this strategy is to reduce power consumption and die area by exploiting the great advancements in digital processing. The model of an 8x8 pixel CdZnTe detector and the detector crystal unit are shown in Fig. 1. [7]

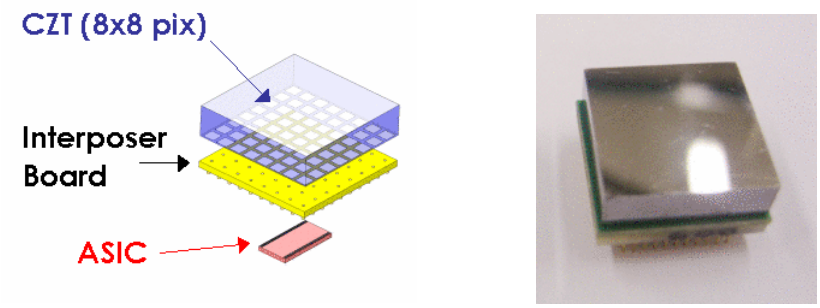

Fig. 1. Model of CdZnTe detector and detector crystal unit (from NASA)

This paper presents a continuous-time delta sigma ADC especially designed for direct analog to digital conversion of CdZnTe detector arrays. In Section II, the proposed concept for direct analog to digital conversion is described. Section III presents the behavioural modeling of the delta-sigma modulator and the circuit level implementation of each building block. Section IV shows simulation results and layout of ADC. The paper closes with a summary in Section V.

II. Direct conversion concept for CdZnTe detector arrays

Readout circuits for CdZnTe detector arrays measure charges caused by electron-hole pairs generation due to ionizing events. These circuits are mainly based on semi-gaussian shaping of the input signal followed by peak height detection and timing analysis in the analog domain [2]. The semi-gaussian shaping has been developed over many years [1] and is up to now used in many detector circuits. A typical detector channel as used in current developments [3] is depicted in Fig. 2. The charge pulse emitted by the sensor is integrated by a charge sensitive amplifier and filtered by shaping filters. Peak sampling or timing analysis can be done on the shaped pulses depending on the selected shaping time.

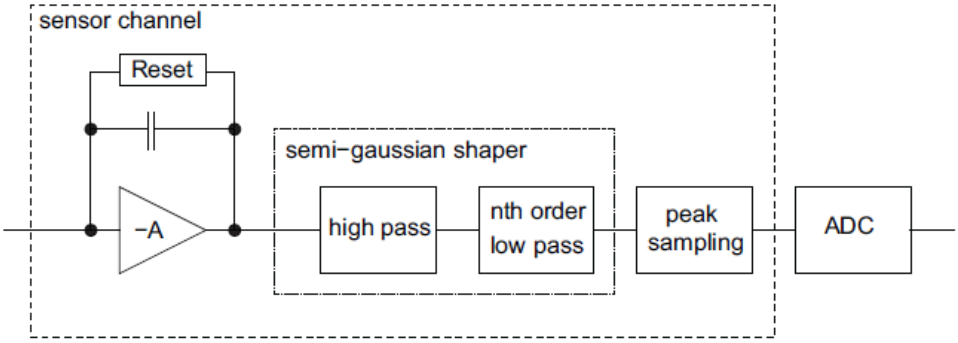

Fig. 2. Conventional channel architecture (the ADC is shared by multiple channels)

Fig. 3 depicts the described signal processing chain. The analog shaping filters in front of the sampling circuit are required to avoid aliasing during the sampling process and to suppress high frequency noise. Relaxed requirements in terms of anti-alias filtering would offer the possibility to move pulse shaping, peak detection and peak sampling into the digital domain. Continuous-time (CT) delta-sigma ADCs fit very well into these requirements:

- The shaping filters can be moved to the digital domain due to the implicit anti-alias filtering of these converters.
- The resolution scales with the data rate which makes it a perfect solution for high data rate timing analysis as well as high resolution peak sampling.
- The digital processing can be easily shared between several pixels.

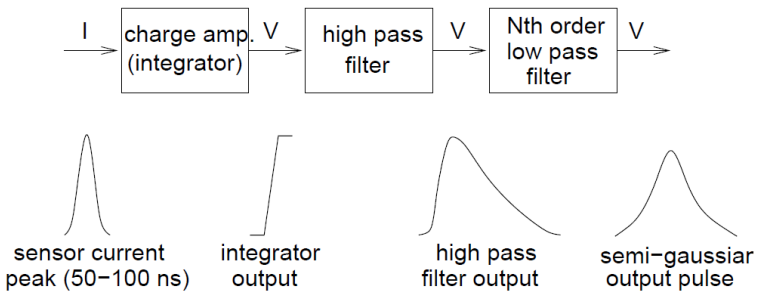

Fig. 3. Conventional signal processing chain

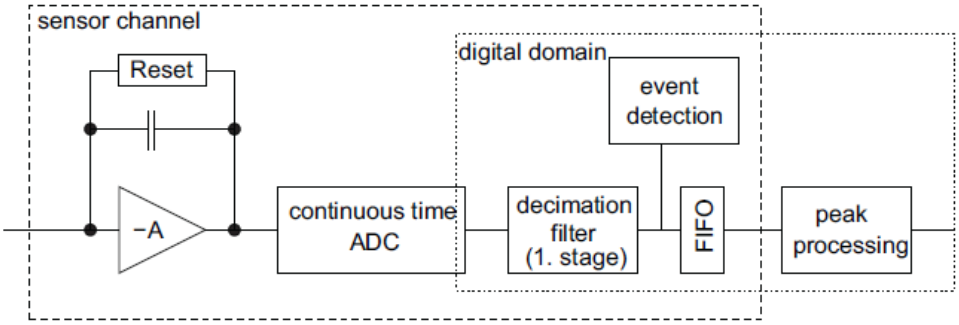

Fig. 4. New proposed channel architecture

This paper presents a new architectural approach for an early analog to digital signal conversion in a multi channel gamma ray detection system. A continuous-time delta-sigma ADC was especially designed for direct analog to digital conversion of CdZnTe detector arrays. Fig. 4 shows a block diagram of the channel architecture of the new approach.

III. Behavioral modeling and circuit level implementation

There are various architectural choices in the design of a CT delta-sigma modulator. The performance of the ADC can be optimized by appropriate selection of the loop filter transfer functions, the modulator order and the number of bits of the quantizer.

A. Topology Selection

The signal processing requirements for CdZnTe detector arrays define the specification for the ADC. The design aim of the peak resolution is 12 bit which results in a minimum SNR of 74 dB. Due to the non-linearity correction in the post process steps the THD can be relaxed to -50 dB. A signal band of 625 kHz is selected to allow every shaping time above 200 ns. Lower shaping times can be achieved with reduced resolution. The generation and distribution of very low jittered clocks on large readout ICs is a challenging task. A multi-bit implementation with non return-to-zero feedback pulses offers the possibility to be tolerant against clock jitter. It also allows a second order loop in combination with an oversampling ratio of 50 which reduces the number of operational amplifiers and the requirement of gain-bandwidth as well. Fig. 5 without the dashed part illustrates the idealized model of such a modulator. A 2nd order integrator and a 4 bit quantizer compose the feedforward path while the feedback path consists of a 4 bit DAC. The gain coefficients k_1 and k_2 amplify the output signal and feed it back to the input of both integrators respectively. Behavioral simulations in Matlab proved that high resolution can be obtained, when k_1 and k_2 equal 1 and 1.5 respectively. The model in Fig. 5 assumes zero delay inside the loop. In reality there is a non-zero delay known as excess loop delay which has to be addressed. In case the excess loop delay t_d reaches the same order of magnitude as half of the clock period T_s, the CT modulator becomes unstable. The delay of the quantizer also depends on the input signals and is therefore strongly signal dependent which could introduce harmonics into the loop. To solve this problem, an additional feedback path is introduced and the delay is forced to a fixed value, as illustrated in the dashed part in Fig. 5 [4]. This path is applied directly to the quantizer input and an explicit time delay t_d is added. Assuming that $t_d = 0.5T_s$, the feedback coefficients are:

$$a_1 = 1$$
$$a_2 = 2$$
$$a_3 = 0.875$$

The implementation of gain coefficients based on RC time constants strongly depends on process variations. Extensive behavioral simulations show that the modulator remains stable up to 20 % variation of the coefficients. Digital controlled trimming is used to attenuate the process variations down to this limit.

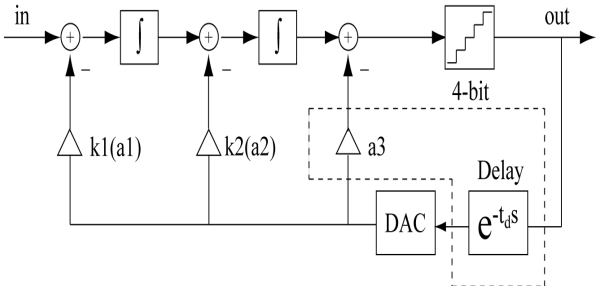

Fig. 5. Modulator model

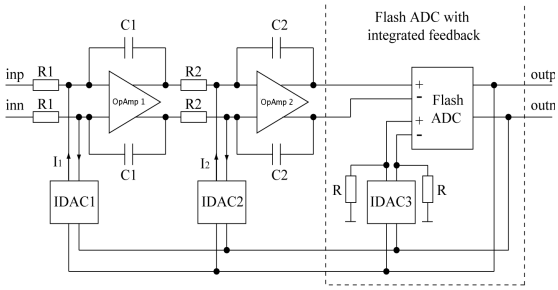

Fig. 6. Modulator block diagram

B. Circuit Implementation

After determing the feedback coefficients a_1 to a_3, the modulator model should be transformed into circuit level. The modulator block diagram is illustrated in Fig. 6. Two RC integrators are implemented for the 2nd order loop filter. The 4 bit quantizer is realized as a flash ADC. Three current-mode DACs (IDACs) feed back the quantizer output to the inputs of the respective building blocks.

Flash ADC with Integrated Feedback: Since the quantizer includes a direct feedback, it is necessary to implement the flash ADC together with the 3rd DAC. In this case a critical point is to implement the summing operation. In order to avoid the complexity of summing two voltage signals at the input stage of the quantizer, the summing operation is shifted to the reference stage. The resulting quantizer exhibits the same signal transfer as achieved by summing at the input nodes. A fixed value is added to the reference voltage by shifting the whole reference resistor string depending on the feedback DAC.

Current mode DACs: The current mode DACs in the feedback loop are located between the flash ADC and the respective integrator. Using a complementary structure and cascoded current source devices, the IDAC cell can precede positive and negative output currents which exhibit complementary values at outp and outn [5]. By combining these currents to the same nodes, the sum of each output current can be obtained for outp and outn respectively.

Loop Filter: Two RC integrators are implemented for the 2nd order loop filter, where the integrator gains are mapped into resistor-capacitor products. To ease the design of the modulator the same amplifier is used in both integrators. Due to the fact that the performance is mainly limited by the first one, the second amplifier can be sized down to reduce power consumption. The OpAmps employ two stage design using Miller compensation. For the first amplifier stage a local CMFB is used. It provides additional gain boosting and increases the slew rate as well as GBW of the amplifier. In the second stage, a SC-CMFB circuit is employed.

IV. Simulation results and layout of ADC

Architectural block level simulation and optimization were done with HDL-Models. Finally a transient simulation for the overall delta-sigma modulator was performed on circuit level. The clock was set to 50 MHz with a duty cycle of 50 %. A sine signal with 0.6 V amplitude (-4.4 dBFS) and 500 kHz frequency was applied. The output data of the modulator were exported to Matlab to compute the spectrum using a 4096-point Hanning windowed FFT. The spectrum of the output data is depicted in Fig. 7. Further transient simulations were performed with sweeping the input signal amplitudes. The resulting SNR versus the normalized input amplitude is shown in Fig. 8. Maximum SNR is simulated at 0.7 V input amplitude (-3 dBFS) and equals 78.3 dB. The calculated Dynamic Range (DR) is 81 dB.

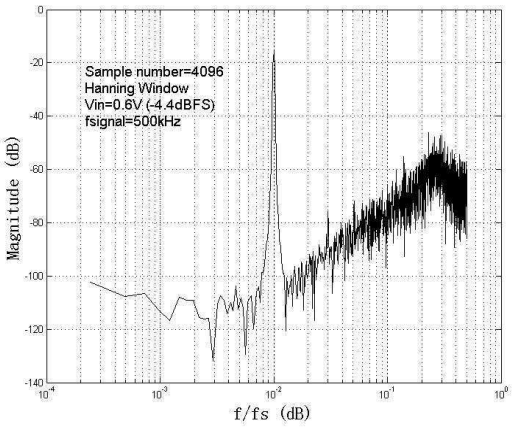

Fig. 7. Power spectrum density

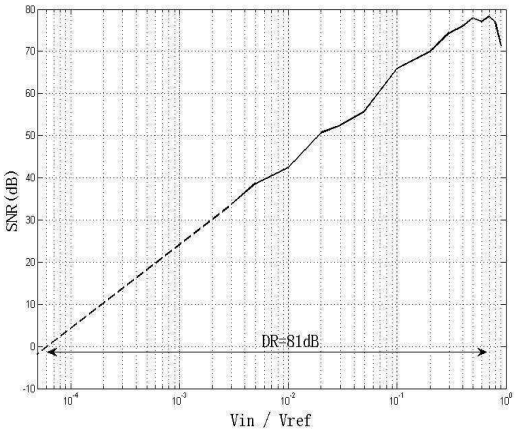

Fig. 8. SNR versus input amplitude

The main performance parameters of the delta-sigma modulator are summarized in Table I.

signal bandwidth	625 kHz
sampling frequency	50 MHz
oversampling ratio	50
dynamic range	81 dB
SNR	78.3 dB
SNDR	57.5 dB
supply voltage	1.8 V
power consumption	3.78 mW
Technology	0.18 μm CMOS

Table I. Performance summary

In the next step a layout of the whole modulator was accomplished and it provides a good matching performance within a 1.5x1.5 mm^2 die area. Fig. 9 illustrates the layout of the continuous time delta-sigma ADC. The prototype chip is currently in fabrication.

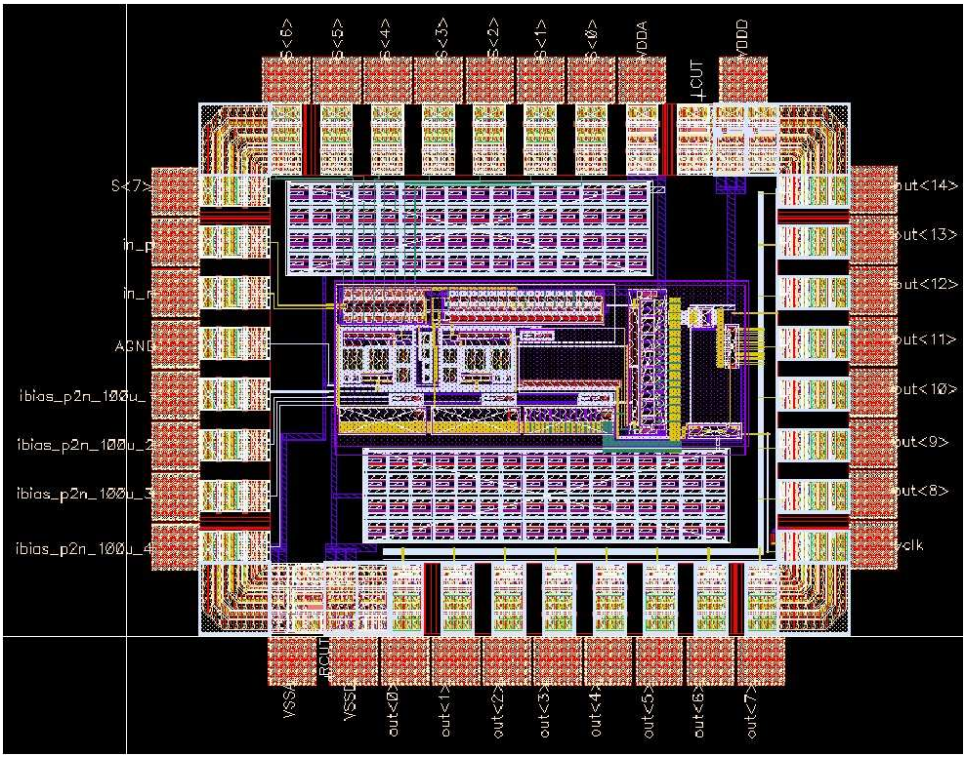

Fig. 9. Layout of the continuous time delta-sigma ADC

V. Summary

This paper covers the design and implementation of a continuous time delta-sigma ADC for a new readout strategy of CdZnTe detector arrays. A 2nd order loop filter associated with a 4 bit quantizer and current-mode feedback DAC were chosen. In behavioral modeling, the critical excess loop delay problem was addressed by means of a local feedback loop. The quantizer was based on a flash-ADC and integrates the local feedback loop. HDL-modeling simulation was used to verify the architectural function. Through circuit level simulations, the output signals were obtained and processed in Matlab. The SNR of the overall delta-sigma modulator is 78 dB and the DR is 81 dB within 625 kHz bandwidth. Clocked at 50 MHz, the modulator consumes 3.8 mW power from 1.8 Volt supply.

Literatur

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