Power Electronics Packaging at Fraunhofer IISB

Double Sided Cooling, Selectively Sintering, Ceramic Embedding and more

FRAUNHOFER Institute for Integrated Systems and Device Technology (IISB)

POWER ELECTRONICS

DEVICES AND RELIABILITY

SIMULATION
MATERIALS
TECHNOLOGY AND MANUFACTURING
DEVICES AND RELIABILITY
VEHICLE ELECTRONICS
ENERGY ELECTRONICS

PART OF Forschungsfabrik Mikroelektronik Deutschland

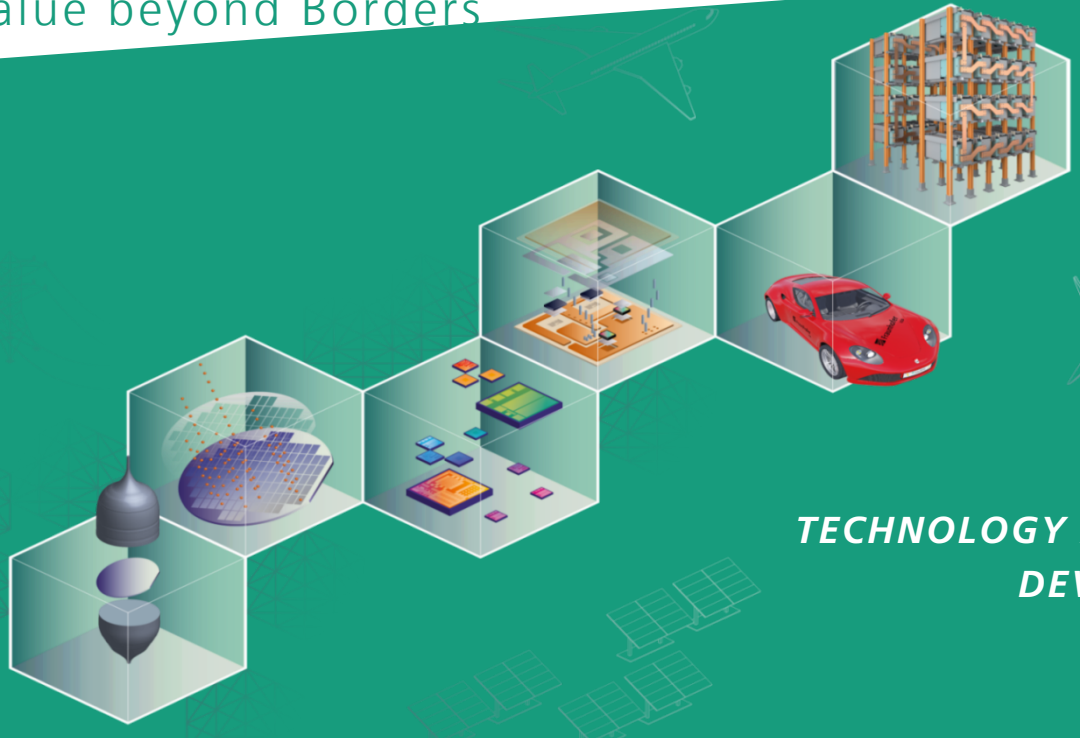
Fraunhofer MIKROELEKTRONIK

FRAUNHOFER IISB – FIELDS OF COMPETENCE

POWER ELECTRONIC SYSTEMS

From Material to Power Electronic Applications

Create Value beyond Borders



SIMULATION
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Fraunhofer MIKROELEKTRONIK

DEVICES AND RELIABILITY

Fields of Competence

From Material to Power Electronic Applications

Tobias Erlbacher

Christoph F. Bayer

Andreas Schletz
Head of Department

Devices → **Packaging** → **Test and Reliability**

Over 30 employes and about 30 students

PART OF Forschungsfabrik Mikroelektronik Deutschland

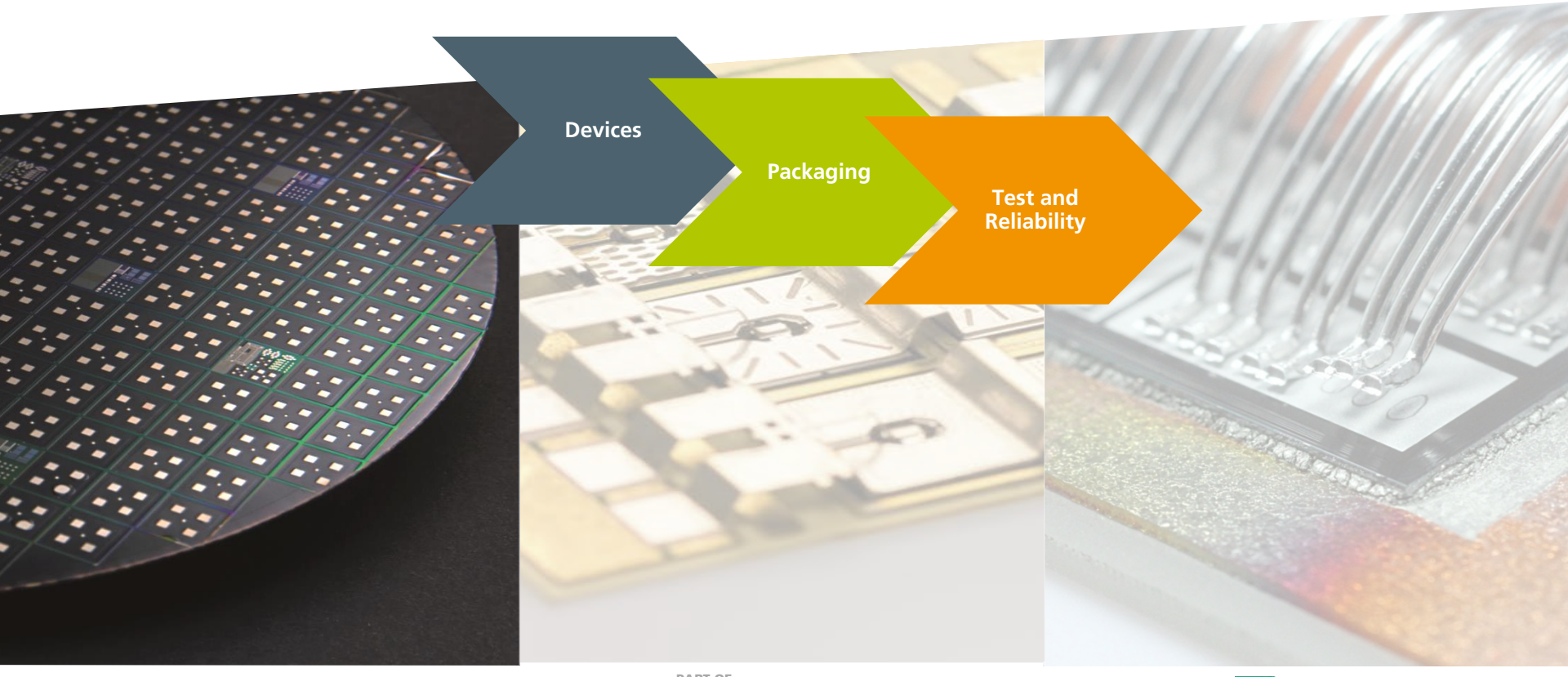
Fraunhofer MIKROELEKTRONIK

FRAUNHOFER IISB - DEPARTMENT

PACKAGING AND RELIABILITY

- New concepts and materials for packaging
- High performance joining technologies, sintering
- Thermal, electrical, and mechanical characterization
- Lifetime characterization, statistical analysis
- Analysis of failure mechanism
- Lifetime modeling

DEVICES AND RELIABILITY



DEVICES

Prototype Fabrication: Access to π-Fab®

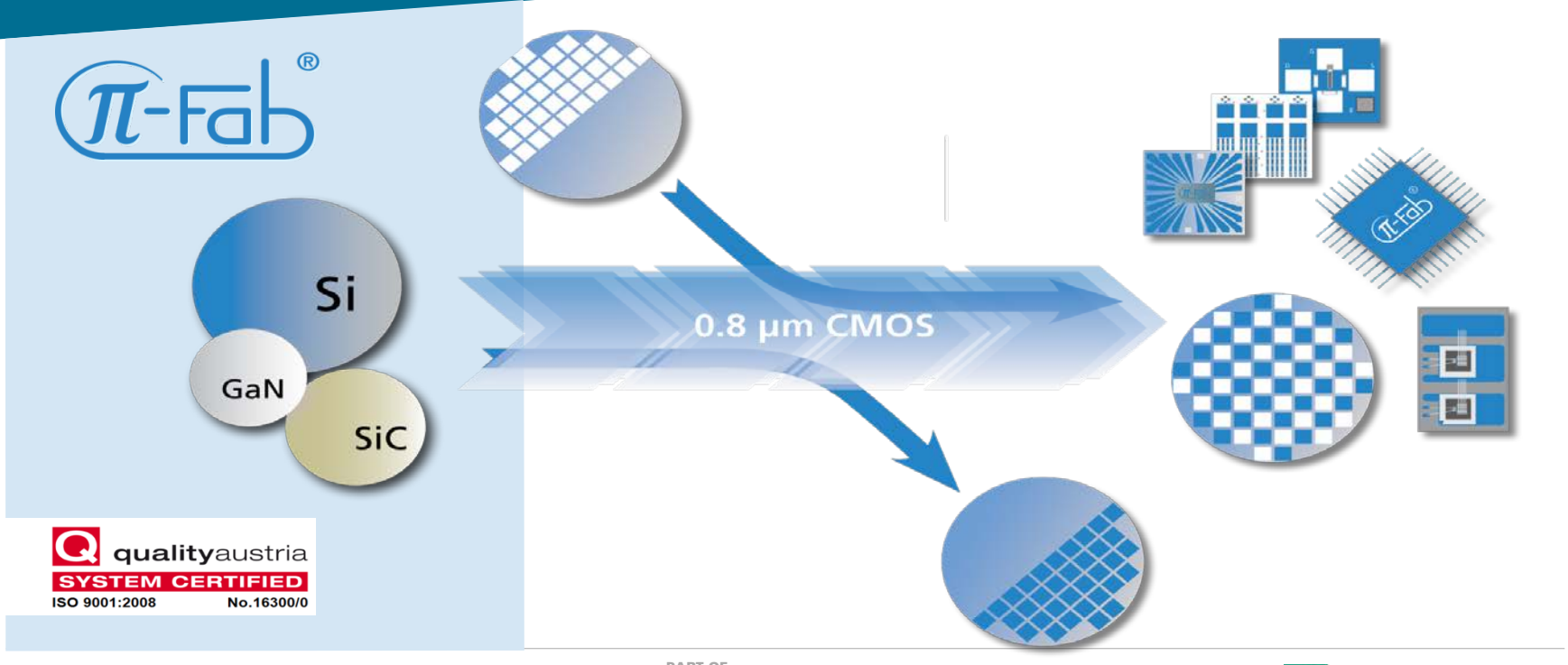
Fabrication of SiC-devices qualified (ISO 9001) processing environment

- Foundation: 200 mm silicon CMOS line
- Upgraded to: 150 mm SiC pilot line

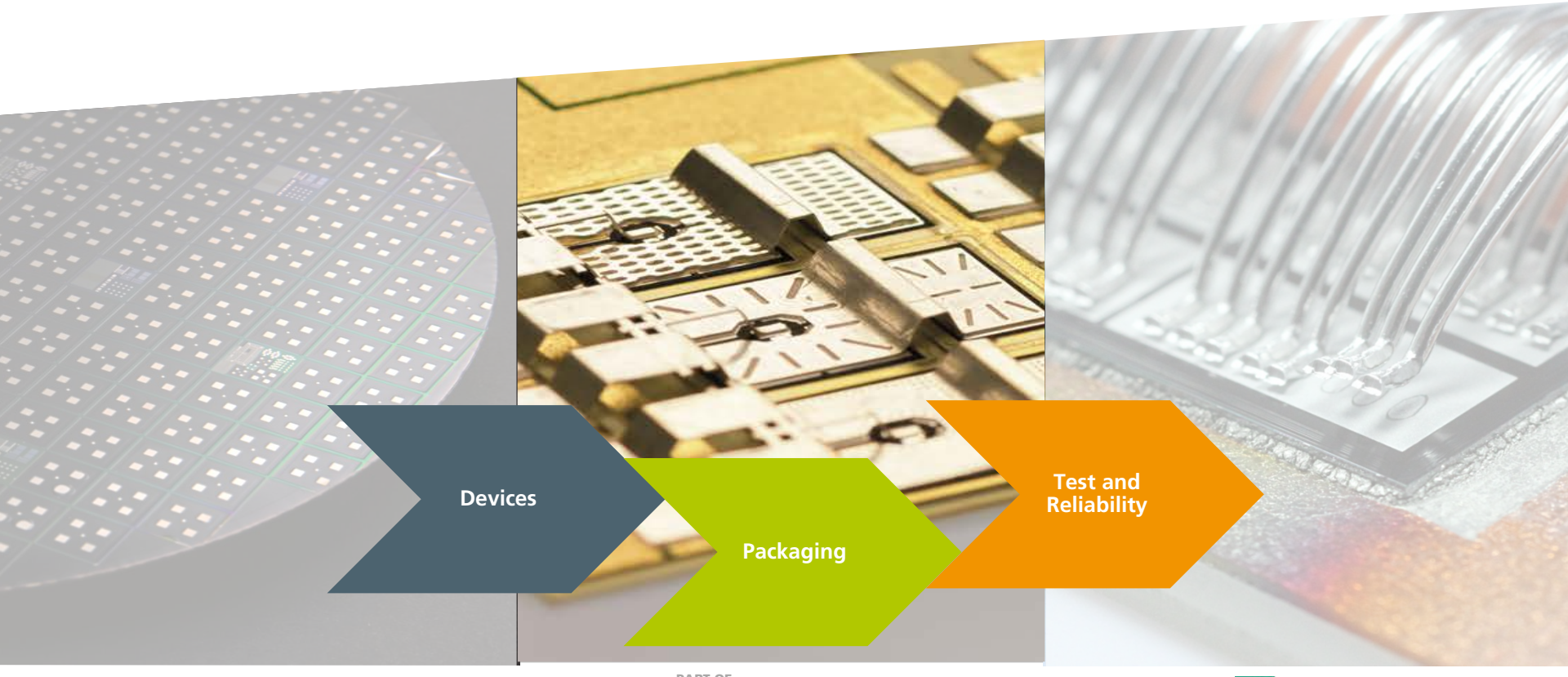
qualityaustria
SYSTEM CERTIFIED
ISO 9001:2008 No.16300/0

DEVICES

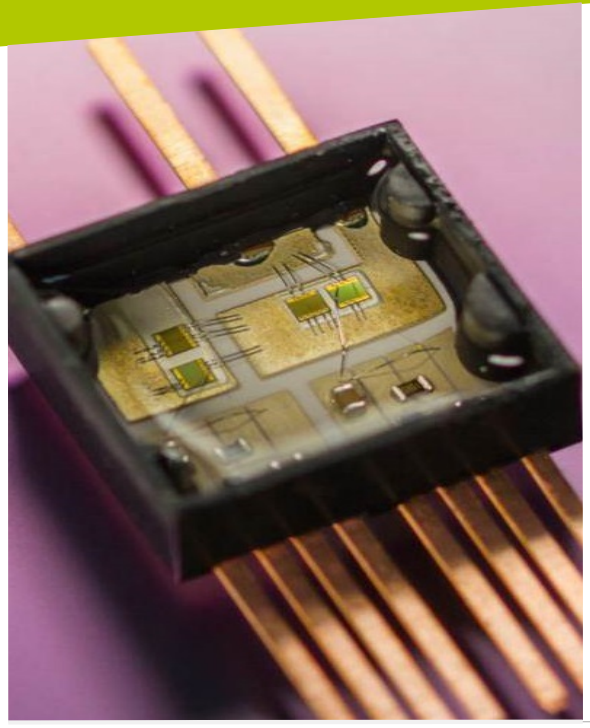
Prototype Fabrication: Access to π-Fab



PACKAGING AND RELIABILITY



PACKAGING
Power and Signal Electronics



Power and Signal Electronics

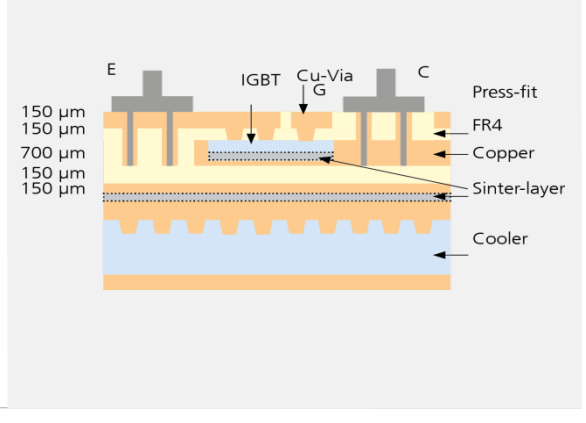
- GaN and SiC power devides
- Integrated gate driver
- Low parasitics
- Silver sintered die-attach for power devices
- High rel. bond wires
- Extended lifetime
- Substrate with metallization for power and signals

PACKAGING

Sintering on Leadframe for Chip Embedding

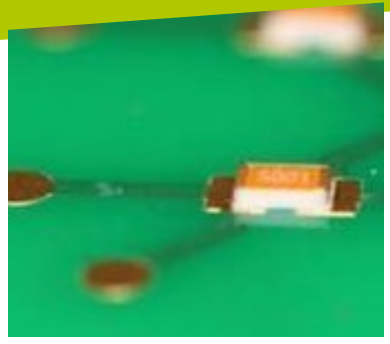
Sintering on Leadframe

- Selective sintering process
- Printing
- Drying
- Chip pick and place
- Transfer to die backside
- Pick and place into cavity
- Final sintering by die servo press



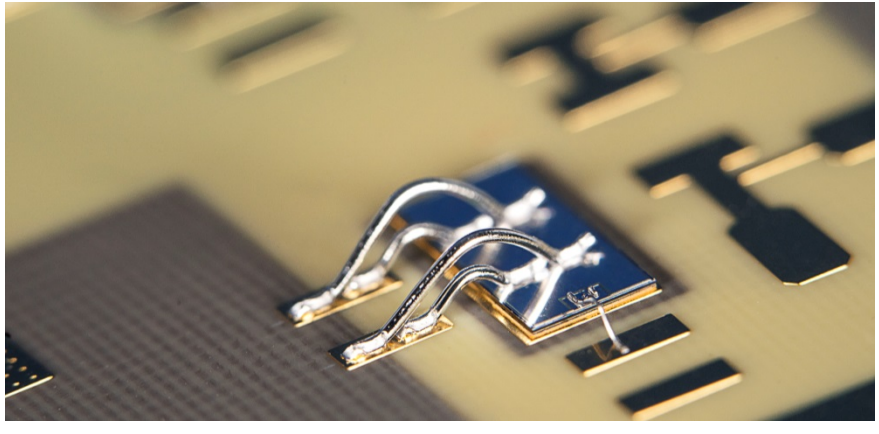
R. Randoll, W.Wondrak, A.Schletz: Dielectric Strength and Thermal Performance of PCB-Embedded Power Electronics, ESREF 2014

PACKAGING
Selective Sintering on PCB



Sintering of Bare Die or SMD Devices on pre-populated Circuit Boards

- Selective sintering process
- Printing
- Drying
- Chip pick and place
- Transfer to die backside
- Pick and place
- Final sintering by die placer



PACKAGING

Top Side Chip Contact

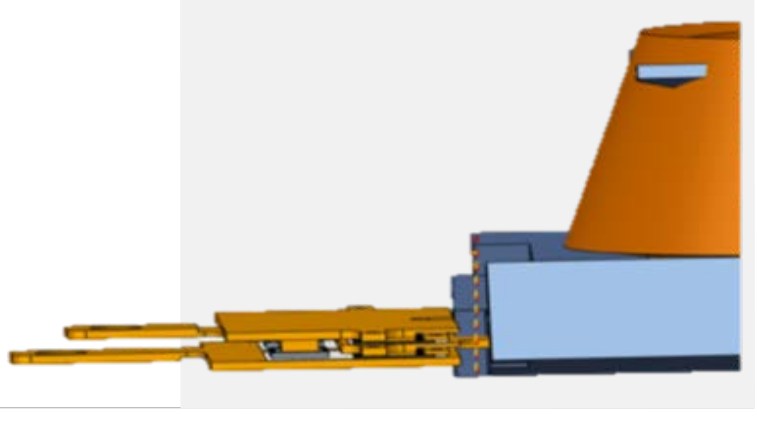
Top Side Leadframe

- Ag-Sintering
- Pressure less process
- Stress relieving measures

PACKAGING
Top Side Chip Contact

Double Sided Concept

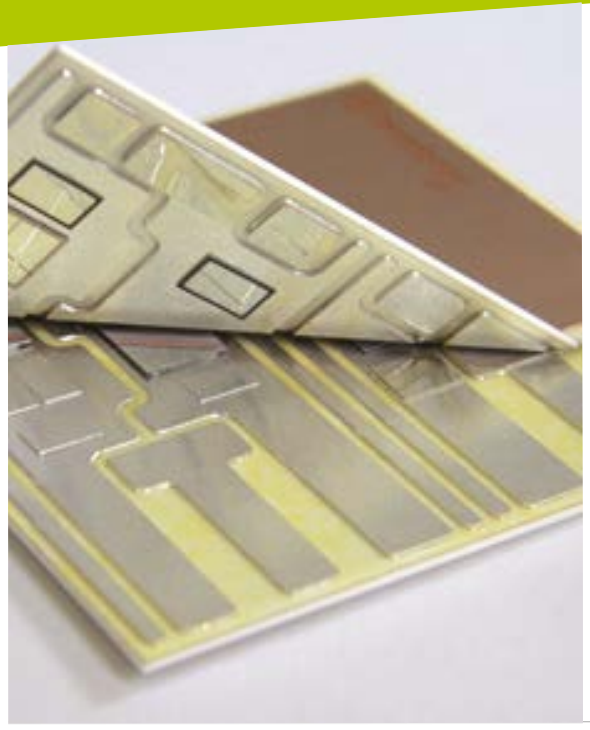
- Full H-bridge
- Chip on busbar



Technologies

- Double sided Ag-sintering
- SiC FET
- Low inductive communication
- Integrated Si-Snubber

PACKAGING
Double Sided Cooling



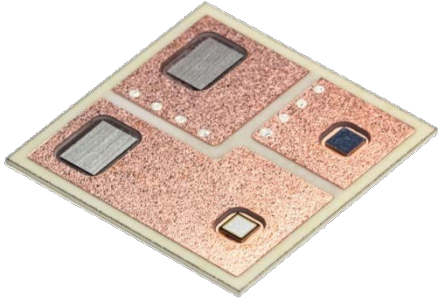
Double Sided Cooling

- R_{th} down to 50 % vs. standard
- Exceptional power density
- Minimum number of different materials
- Non mechanical stress to material stack induced by module fixing or clamping
- Double sided sintered die attach approach

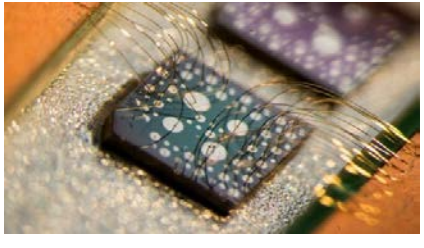
PACKAGING
Ceramic Embedding

Project DiaLe

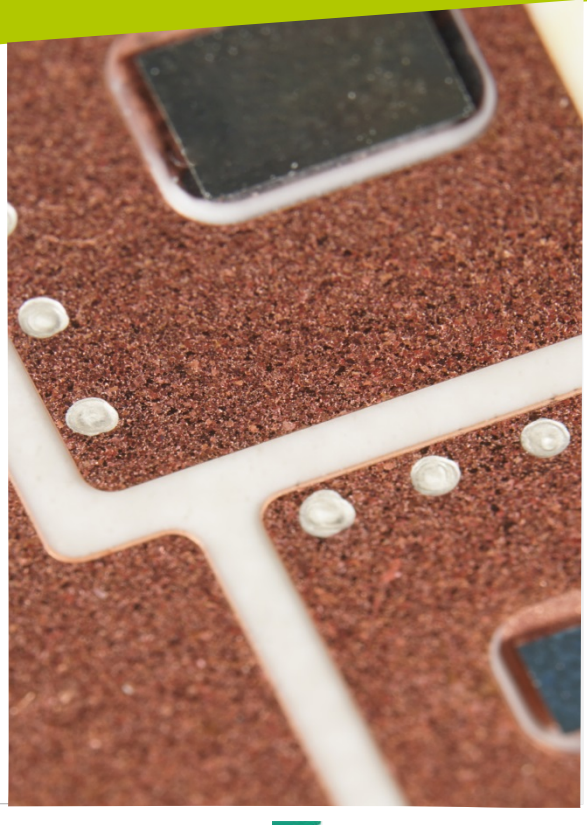
- Diamond for future power electronics applications
- Cooperation of different Fraunhofer institutes
- Diamond wafer manufacture technology for the development of diamond based devices
- Packaging technologies for WBG devices based on ceramic embedding



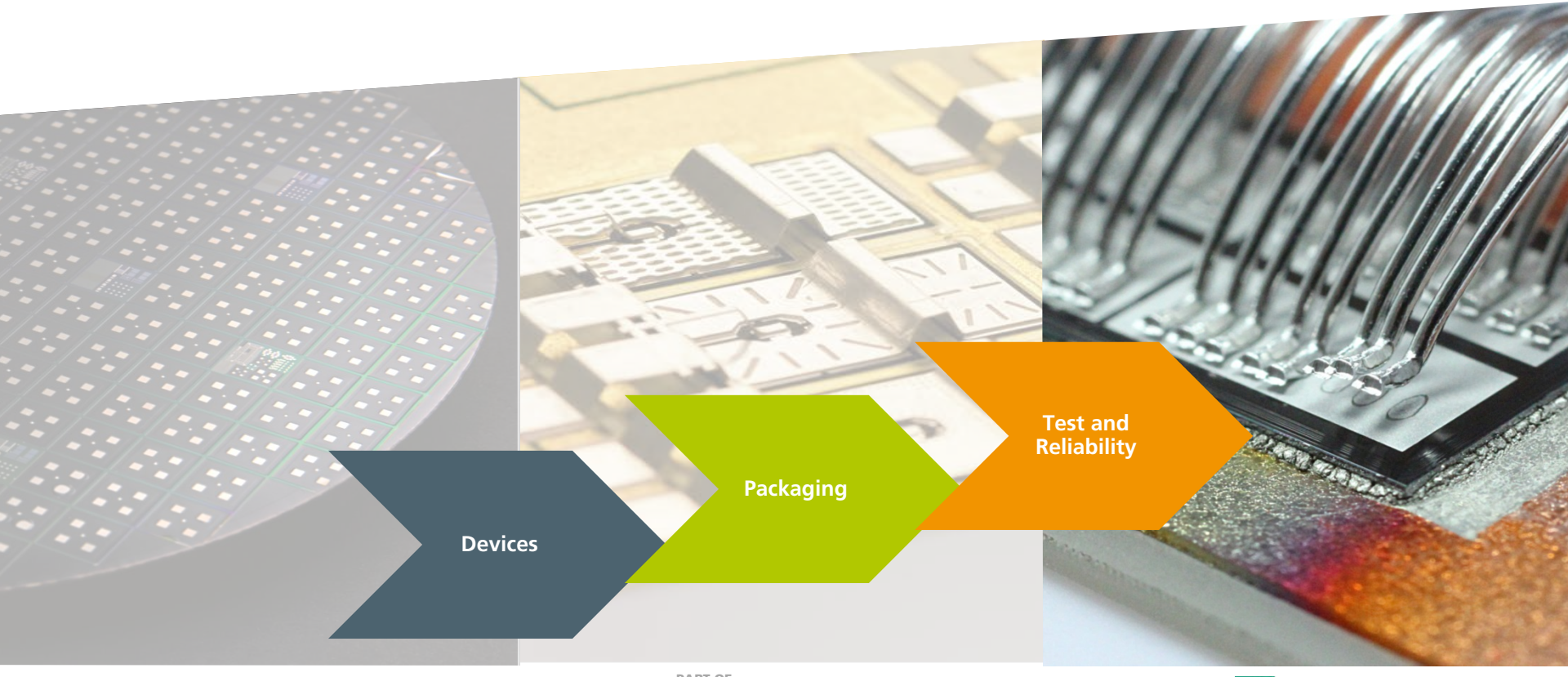
WBG embedded in DBC substrate



Diamond Diodes bonded with Au-wires



TEST AND RELIABILITY



TEST AND RELIABILITY

Test and Reliability

- Active power cycling
- Passive temperature test
- Storage tests (HTRB, H3TRB)
- Corrosive gas test
- Damp heat test
- Statistical analysis
- Test plans and methods
- Lifetime modelling
- Soon: preassure cooker, salt spray, highly accelerated stress test (HAST)

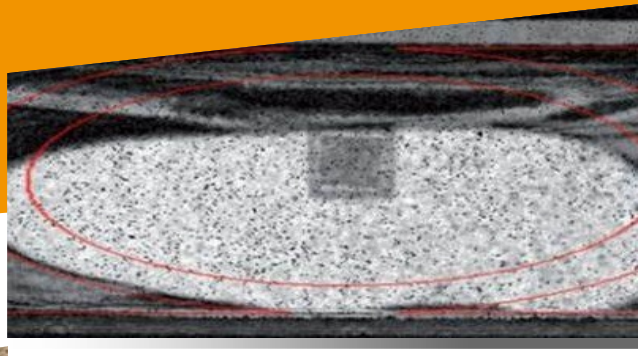
TEST AND RELIABILITY

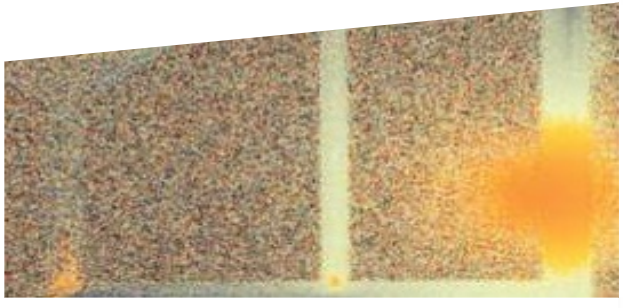
Active Power Cycling Tests

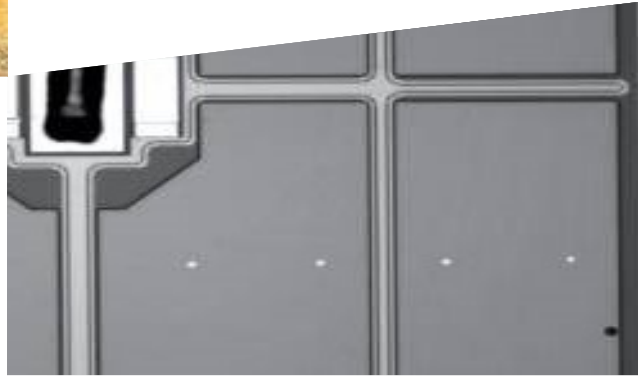
- 5 independent test benches available
- Up to 20 devices in one test run
- On-line measurement and control system for each device under test (indirect measurement principle)
- Thermal impedance Z_{th} measurement during each cycle and all samples

- Individual setting of gate-voltage for every device under test
- Automatic end-of-life-detection
- Heating current from 0.1 A up to 2000 A
- Heating voltage up to 35 V
- Heating and cooling power up to 20 kW
- Coolant temperatures from -60.. +350 °C

TEST AND RELIABILITY
Non-Destructive Analysis



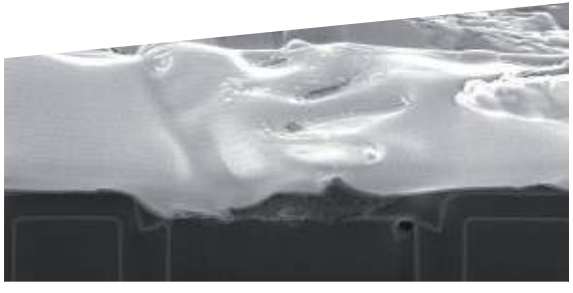




Non-Destructive Analysis

- Optical microscopy
- Ultrasonic microscopy
- Lock-in thermography
- Laser profilometry
- Measurement of electrical parameters

TEST AND RELIABILITY
Destructive Analysis



Destructive Analysis

- Cross section
- Shear and pull tests
- FIB-preparation
- Partial discharge measurement
- STA (DSC+TGA), TMA
- Nanoindentation

THANK YOU FOR YOUR ATTENTION!

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