SIC DEVICE MANUFACTURING USING ION IMPLANTATION: OPPORTUNITIES AND CHALLENGES

T. Erlbacher

Fraunhofer Institute for Integrated Systems and Device Technology IISB

2019-05-23

RESEARCH AND DEVELOPMENT FOR FUTURE SIC-MICROELECTRONICS

KTH IEEE SEMINAR
STOCKHOLM, SWEDEN

Fraunhofer
IISB

Content

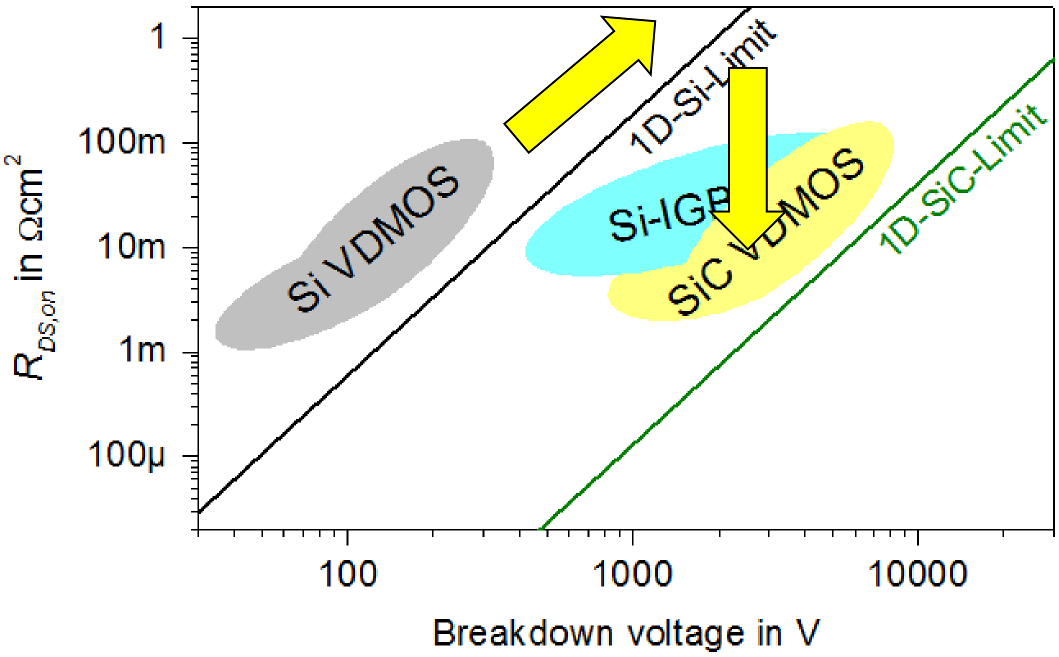
- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Technology push from SiC power devices

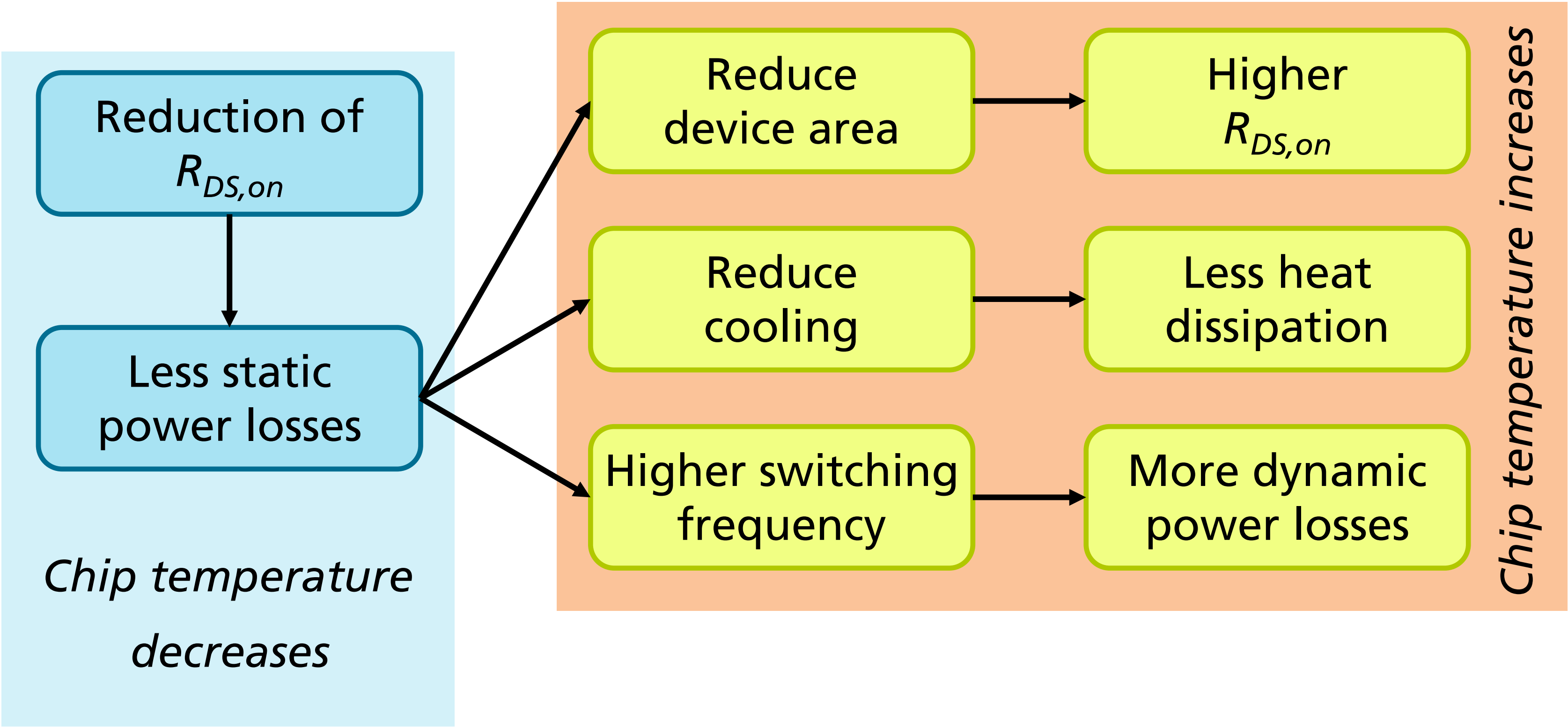
- Reduction of static power losses beyond "state-of-the-art" (Silicon)
  - High critical electric field of WBG material



  - $R_{DS,on}$ of SiC VDMOS transistors similar/superior to Si IGBTs
  - Unipolar instead of bipolar device operation

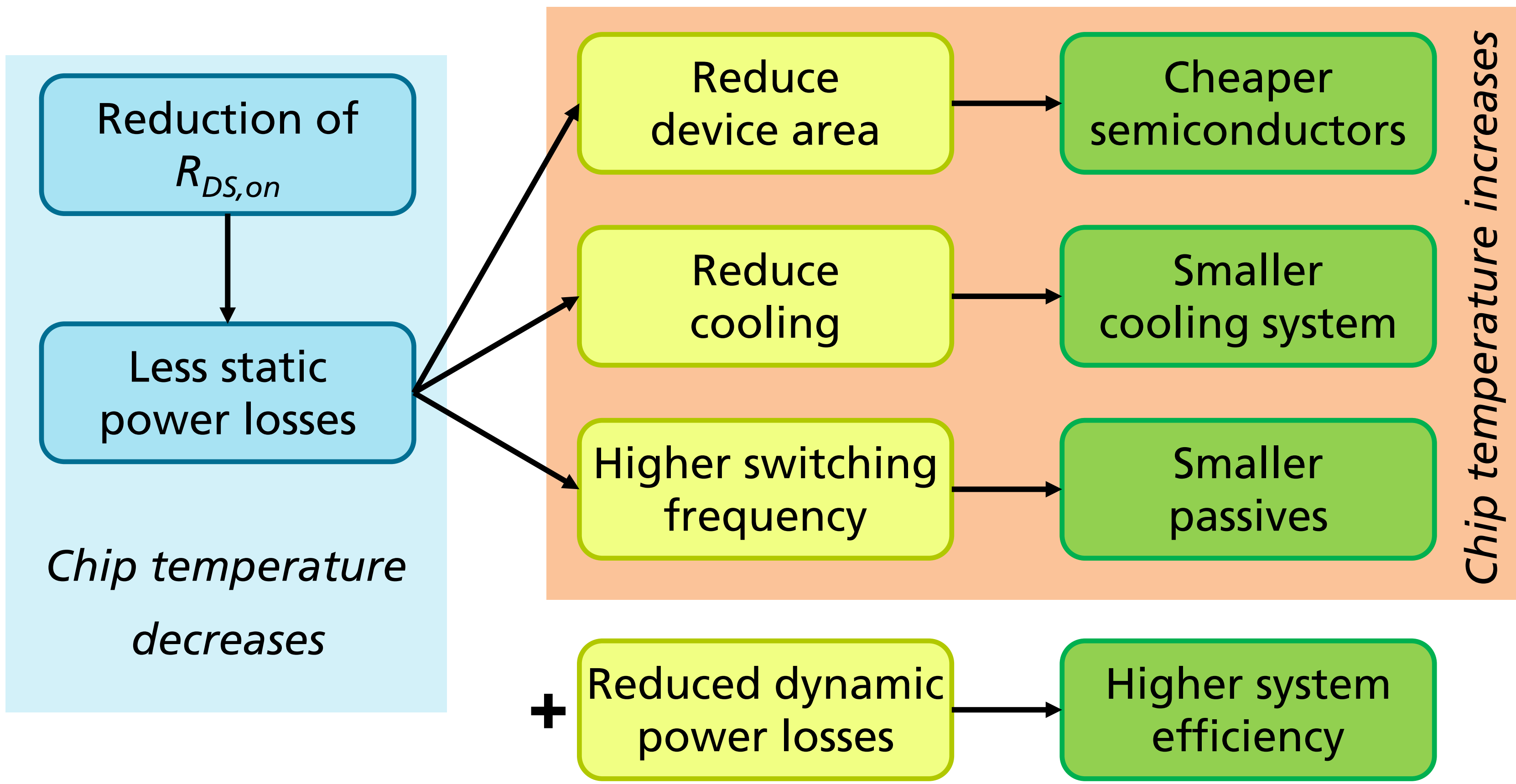
Application pull from power electronics

- Exploitation of SiC device properties in power applications



Application pull from power electronics

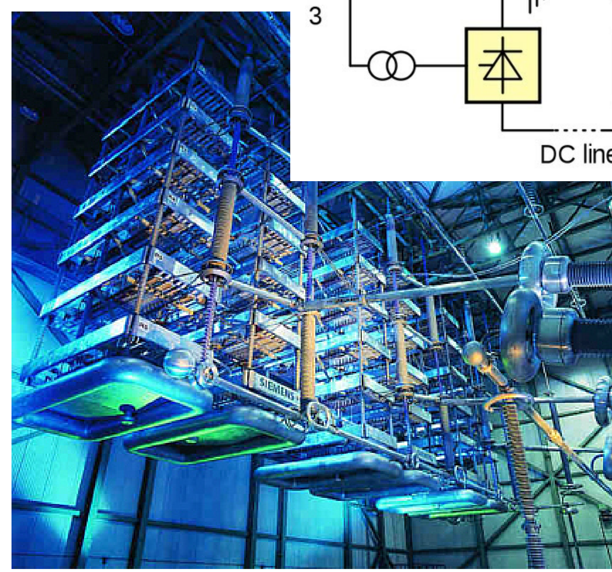
- Exploitation of SiC device properties in power applications

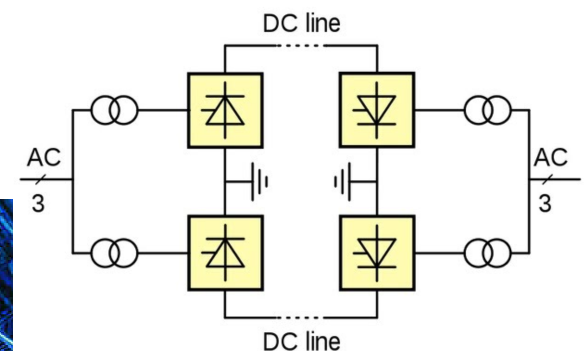


→ "Bill of materials" and CAPEX/OPEX calculations define success for SiC

Application example: High voltage energy transmission

- High voltage solid state transformers and HVDC transmission
  - Benefits of DC-DC transmission
    - Low line losses (inductances and capacitances are not attenuated!)
    - Cheap cables (no AC capable insulation!)
    - Underground cables feasible (regulations!)
  - Solid state transformers required

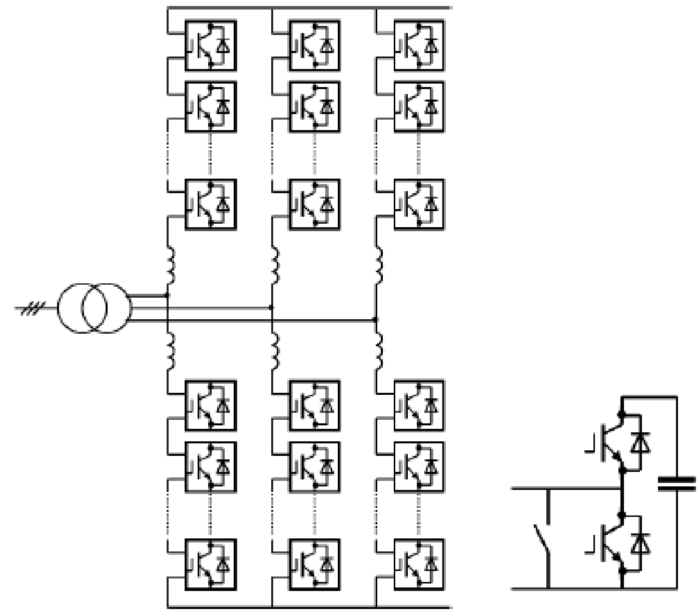




Modular multilevel converter for solid state transformers

- HVDC transmission: No single 380kV power switches available
  - Stacking of several power devices in series to obtain blocking voltage

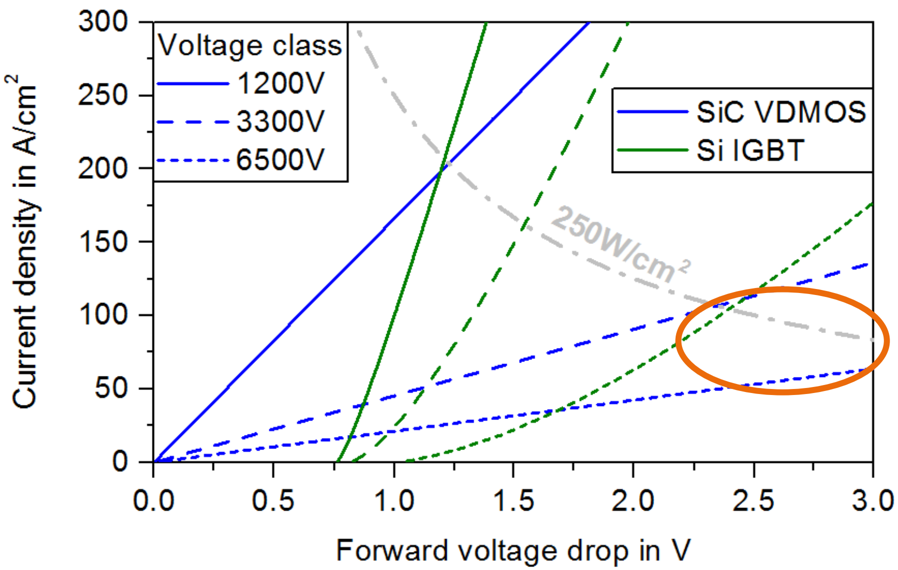
    → Modular multilevel converter topology (commutation cells)

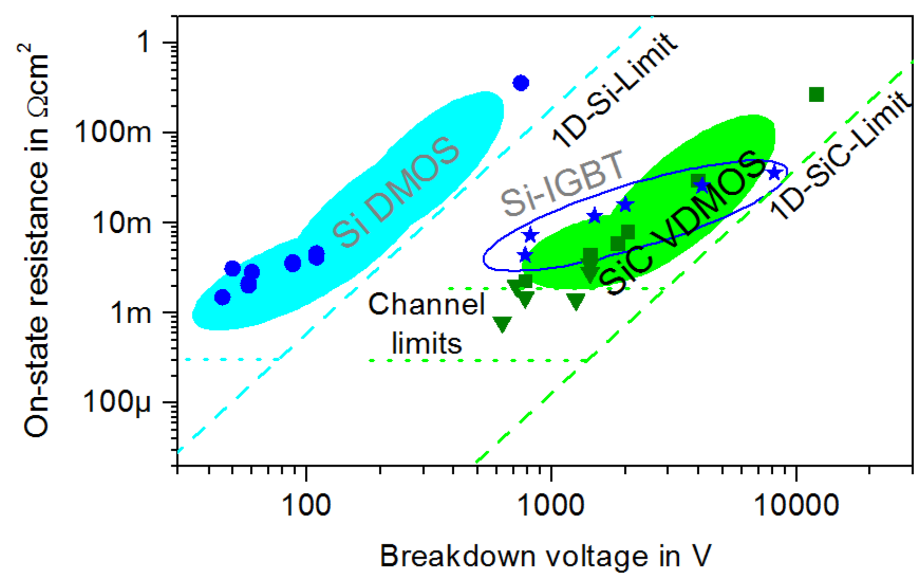


  - Total power losses: Sum of losses in each commutation cell
    - Today: Silicon IGBTs are used, e.g. San Franscisco “TransBay Cable”

High breakdown voltages enabling low power losses

- Benefit of lower static and dynamic losses using SiC devices at 1.2kV:
  - Less forward voltage drop compared to Si IGBT and faster switching





  - But: Diminishing returns for device classes of 4500V and above
  - Si IGBT remains “best-in-class” up to 6.5kV (Si voltage limit)

→ High blocking voltage and low forward losses (conductivity modulation)

Application example: CMOS based electronics

- "Operation under harsh environment" (from a Si CMOS point-of-view)

Energy Industries	Geothermal	Oil & Gas Exploration	Industrial Gas Turbines	Aircraft Engines	Automotive Engines
Required Sensing Temperatures	375°C	275°C	600°C	600°C	300°C
Desired Sensing Measurands	• Pressure • Temperature • H_2S • Strain	• Pressure • Temperature • Hydrocarbon • Strain	• Pressure • Temperature • Flame speed • Acceleration	• Pressure • Temperature • Flame speed • Acceleration	• Pressure • Temperature • Flame speed • O_2

Harsh Environment Sensor Cluster, University of California, San Diego

Power Electronics

Integrated Gatedriver:

- Current
- Temperature

- High switching frequencies
- reliabilty

Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

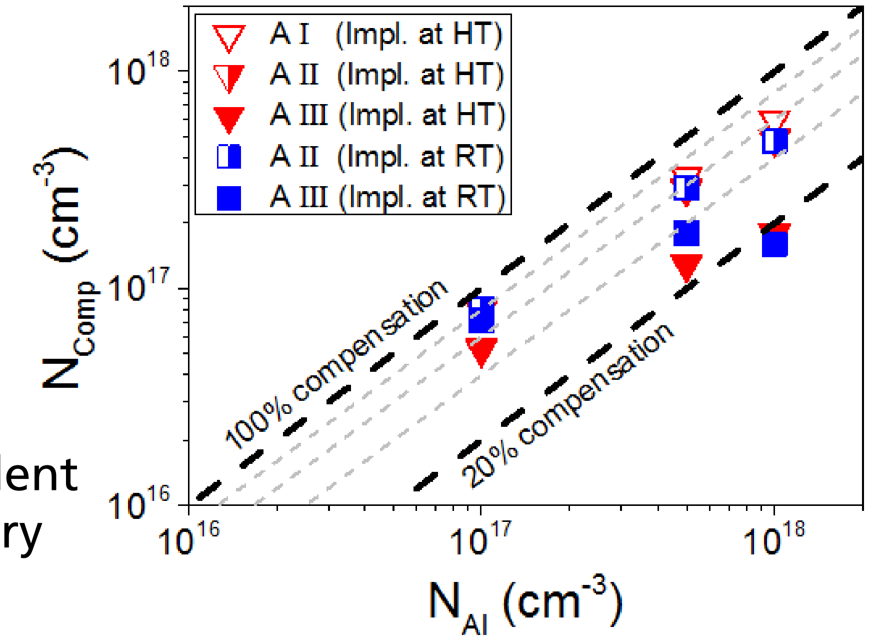
P-Doping in 4H-SiC: Ion Implantation and Annealing

- Fabrication of advanced SiC power devices
  - Ion implantation of Al
  - Annealing of SiC at 1750°C

- SiC p-doping by ion implantation of Aluminum
  - Aluminum is preferred dopant (lowest ionization energy)
  - However, significant charge compensation is observed
    - Up to 90% of implanted ions may be compensated

    → Knowledge of doping dependent Compensation rate manadatory

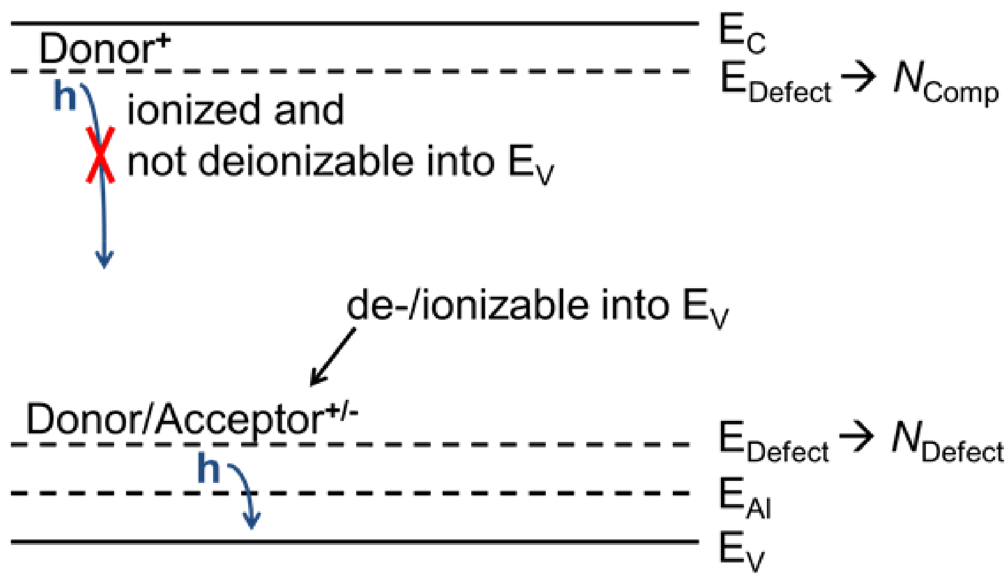
Weisse et al., ECSCRM 2018



Aluminum implantation in 4H-SiC: Compensation

- SiC p-doping by ion implantation of Aluminum
  - Aluminum is preferred dopant (lowest ionization energy)
  - However, significant charge compensation is observed
    - Up to 90% of implanted ions can be compensated

- Analysis of compensation by TLM patterns and DLTS
  - Formulation of defect model

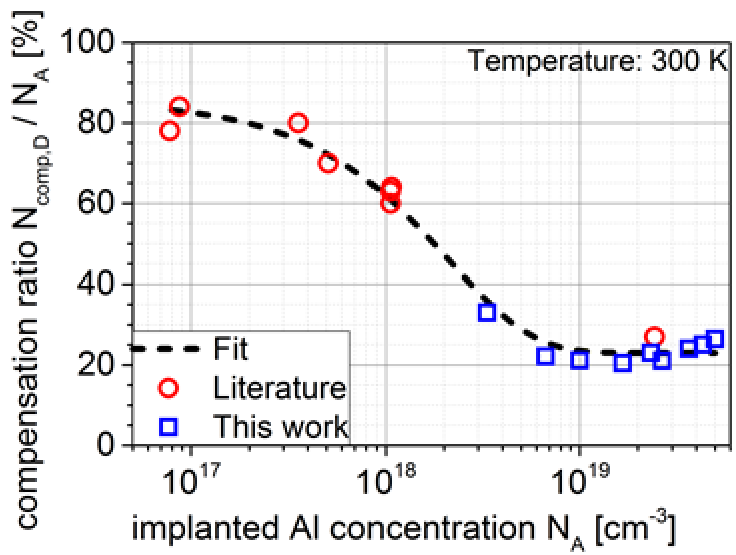


Aluminum implantation in 4H-SiC: Compensation

- SiC p-doping by ion implantation of Aluminum
  - Aluminum is preferred dopant (lowest ionization energy)
  - However, significant charge compensation is observed
    - Up to 90% of implanted ions can be compensated

Kocher et al., ECSCRM 2018

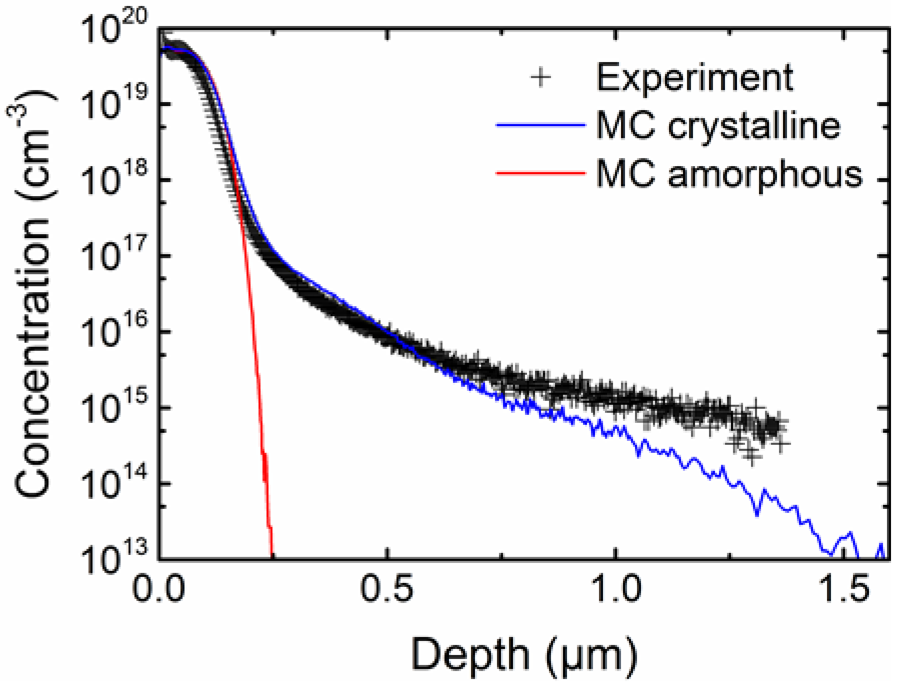
- Analysis of compensation by TLM patterns and DLTS
  - Formulation of defect model
  - Implementation in TCAD modelling
  - Calibration with electrical measurements



Aluminum implantation in 4H-SiC: Channeling

- SiC p-doping by ion implantation of Aluminum
  - Significant channeling and lateral scattering occur
  - Modelling by Monte-Carlo simulation possible

Pichler et al., ECSCRM 2018

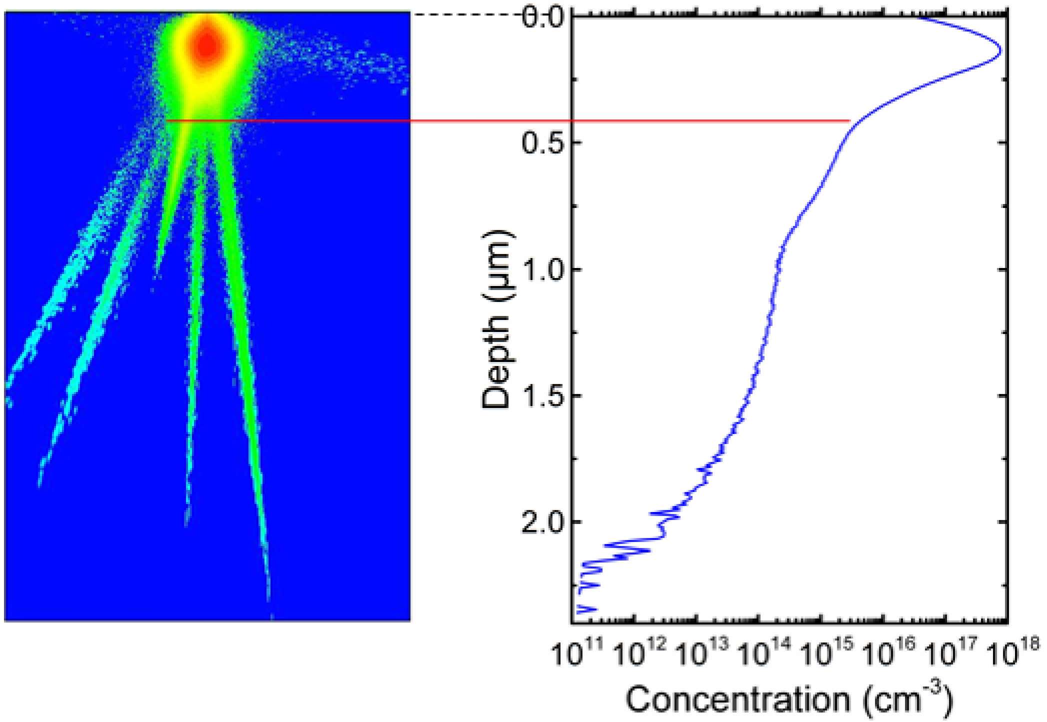


Fraunhofer IISB

Aluminum implantation in 4H-SiC: Channeling

- SiC p-doping by ion implantation of Aluminum
  - Significant channeling and lateral scattering occur
  - Modelling by Monte-Carlo simulation possible
  - Implementation and visualization: TCAD
  - Al Channeling up to 17 times beyond projected range

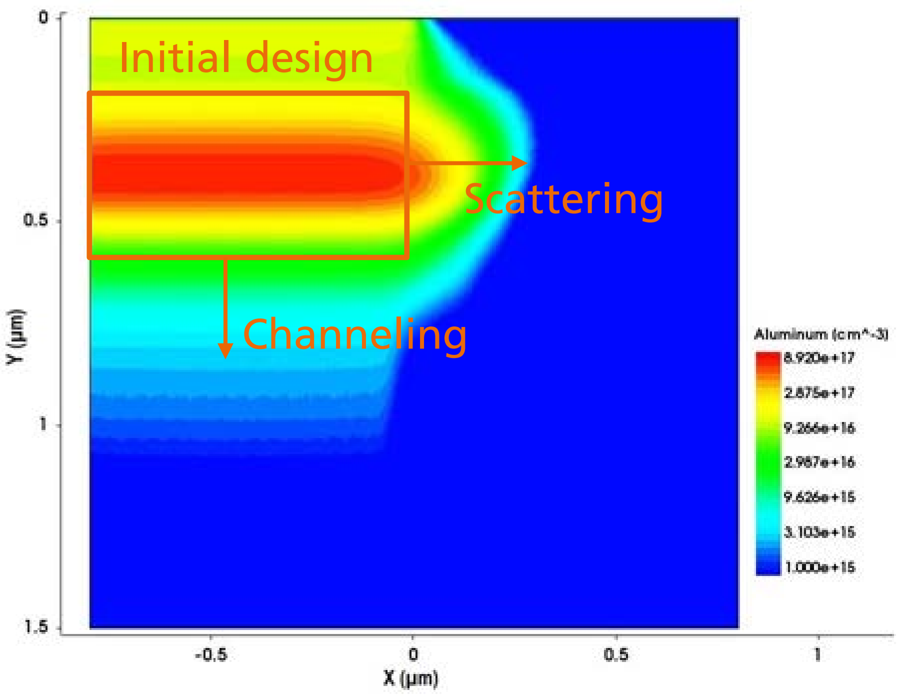
Pichler et al., ECSCRM 2018



Aluminum implantation in 4H-SiC: TCAD modelling

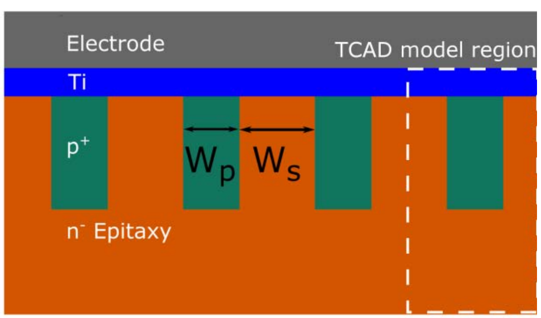
- SiC p-doping by ion implantation of Aluminum
  - Understanding of physical effects enables efficient modelling

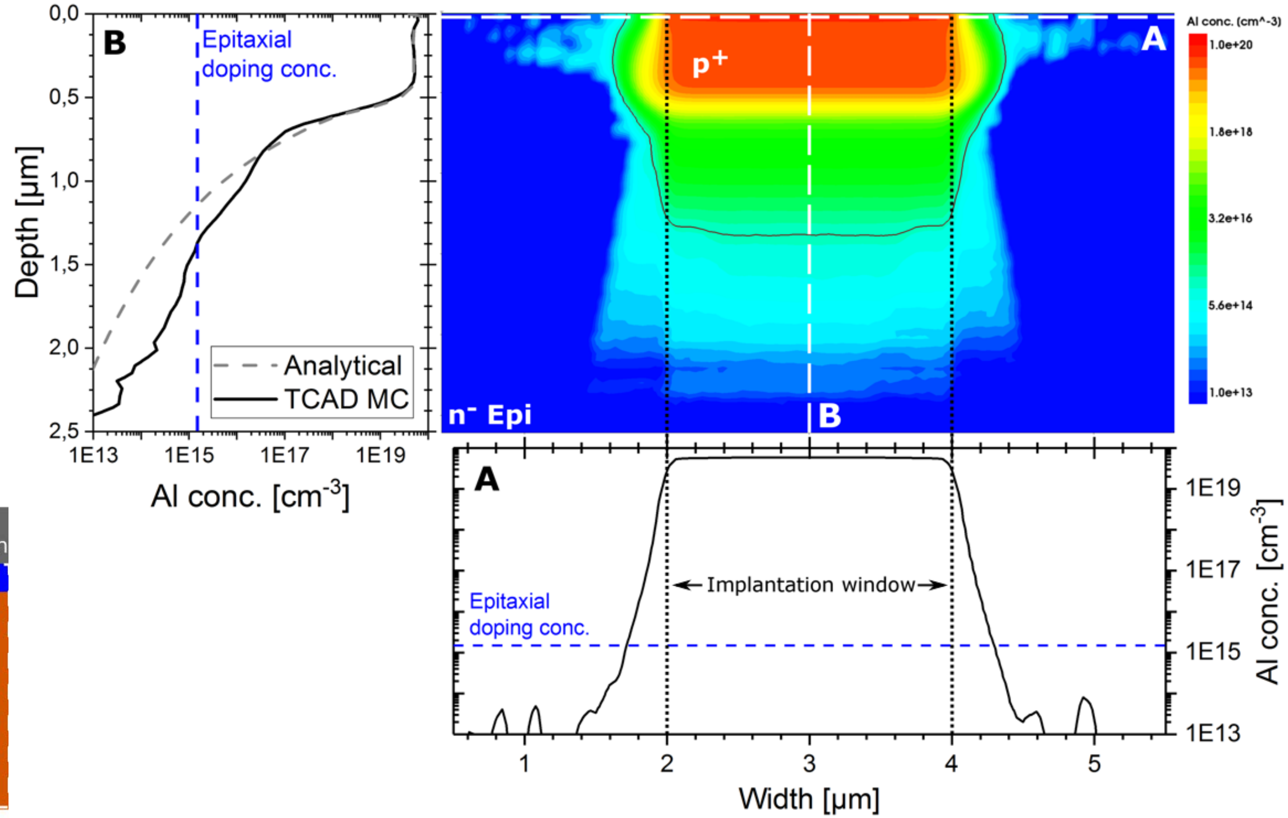
- Example: p-Well implantation for VDMOS transistors
  - Significant deviation from initial expectations
  - Impact on device performance
    - Device resistance
    - Breakdown voltage
    - Threshold voltage
  - Modelling without these effects is not efficient!



Aluminum implantation in 4H-SiC: TCAD modelling

- SiC p-doping by ion implantation of Aluminum
  - Understanding of physical effects enables efficient modelling
- Example:
  JBS Diodes



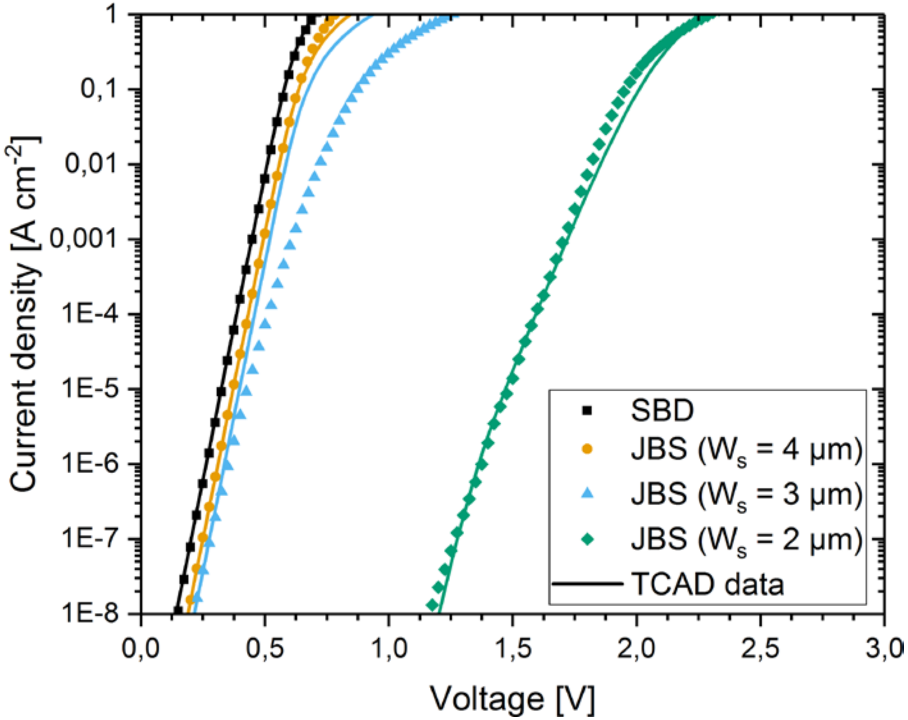


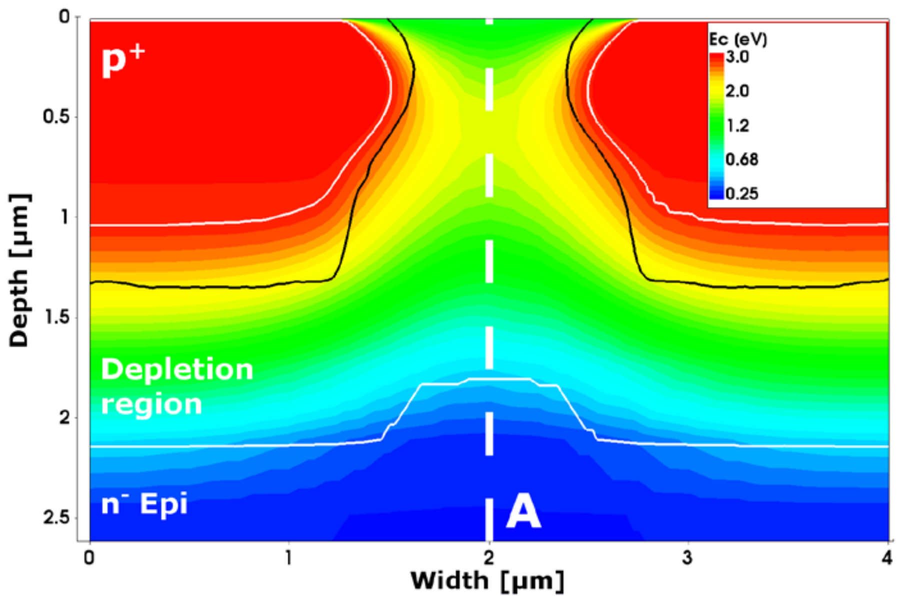
Fraunhofer IISB

Aluminum implantation in 4H-SiC: TCAD modelling

- SiC p-doping by ion implantation of Aluminum
  - Understanding of physical effects enables efficient modelling

Buettner et al., ApplePies 2018



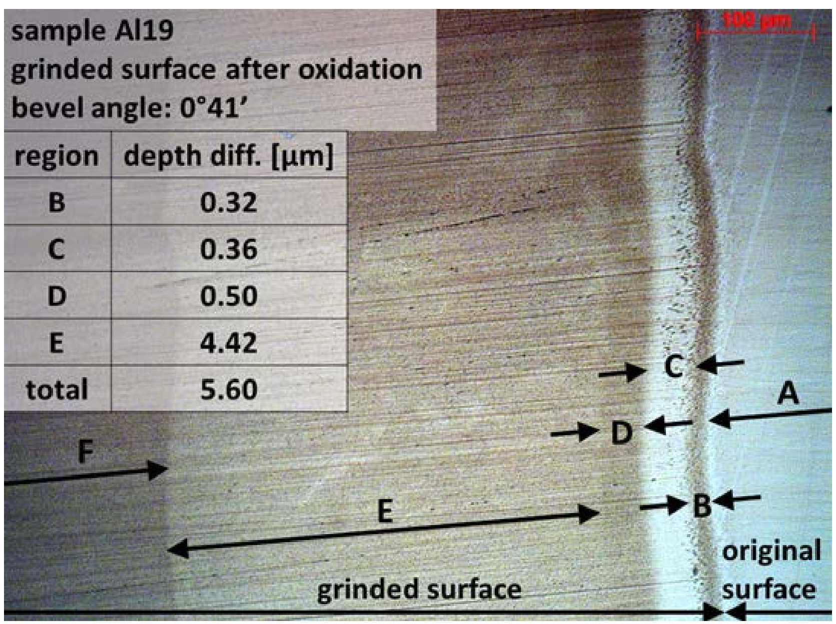


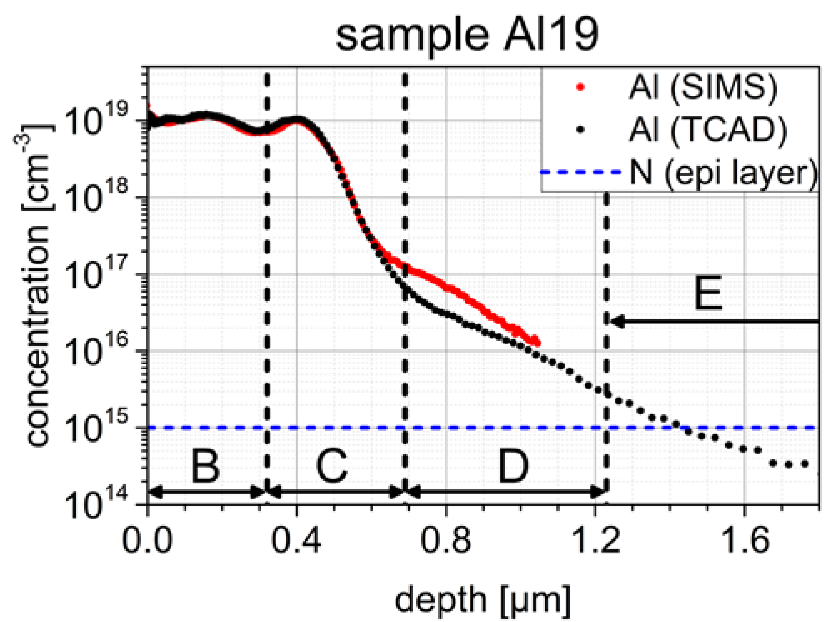
Fraunhofer IISB

Advanced device characterization method

- Investigation of doping profiles
  - SIMS (But: requires calibration samples)
  - Optical profiling using bevel grinding and thermal oxidation
    - Oxidation rate depends on doping concentration

Kocher et. al, ECSCRM 2018

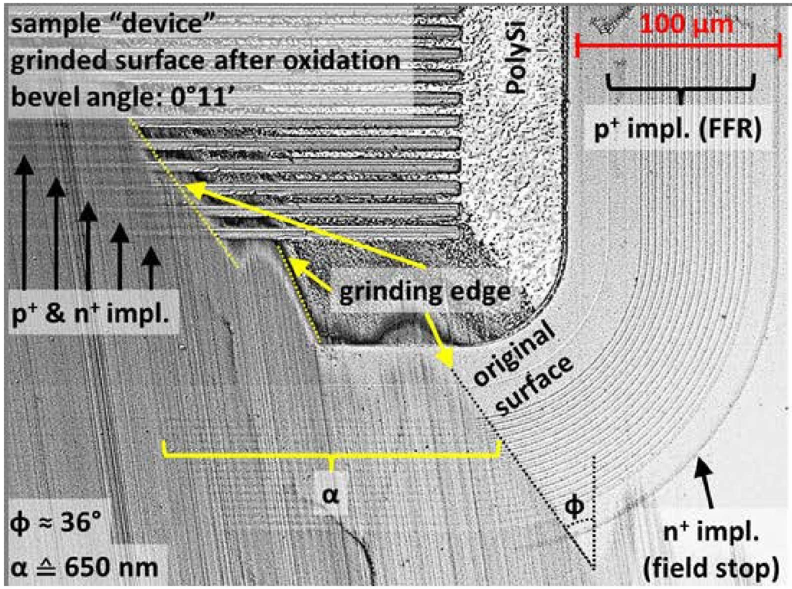


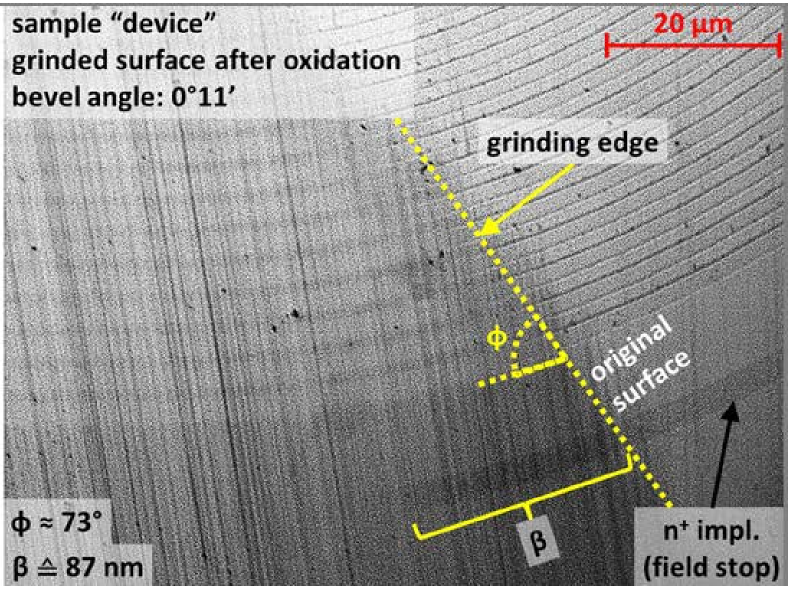


Advanced device characterization method

- Investigation of doping profiles
  - SIMS (But: requires calibration samples)
  - Optical profiling using bevel grinding and thermal oxidation
    - Method also applicable to 3D patterns (e.g. VDMOS):

Kocher et. al, ECSCRM 2018





Fraunhofer IISB

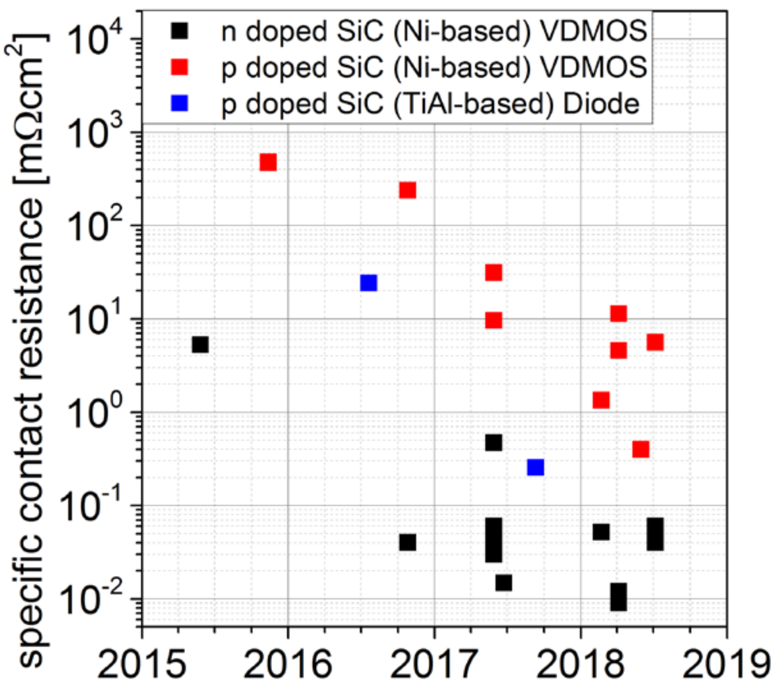
Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Ohmic contact formation

- Improvements of ohmic contact fabrication technology
  - Development of Ni and Ti based contact processes
  - Identification of reaction steps
  - Optimization of processing
    - Al-content in Ti / Ni
    - Optimized RTP conditions
    - Laser annealing

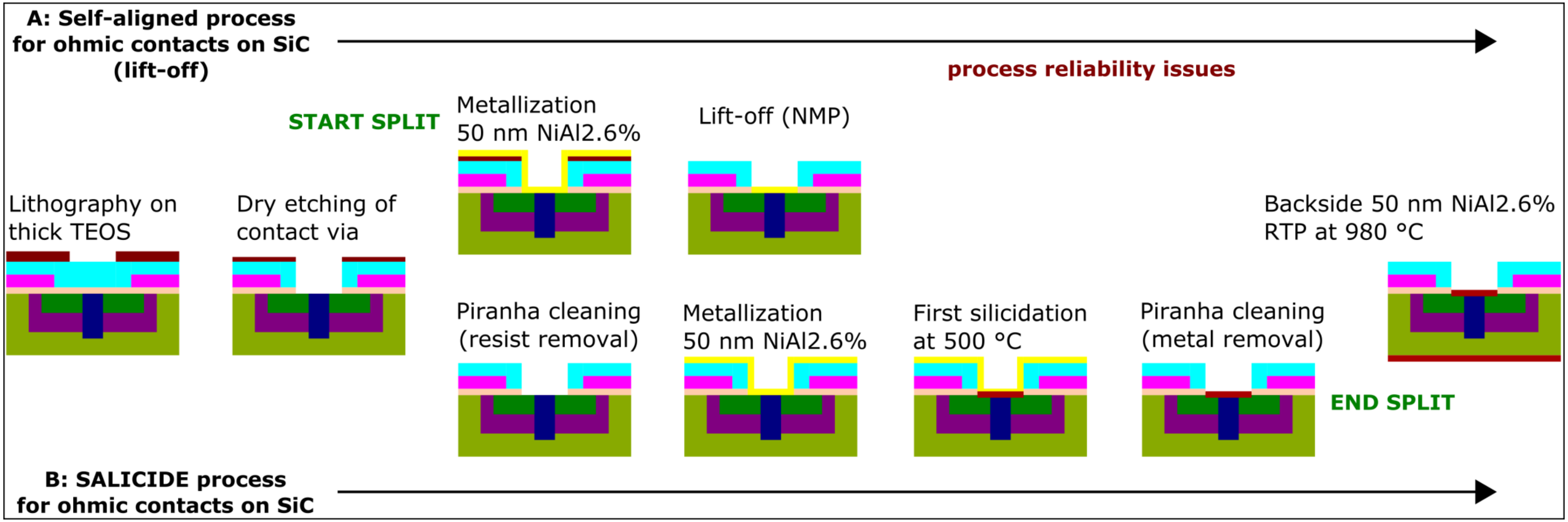
Kocher et al., ECSCRM 2018



Reduction of specific contact resistance for n- and p-doped regions at IISB

Ohmic contact formation

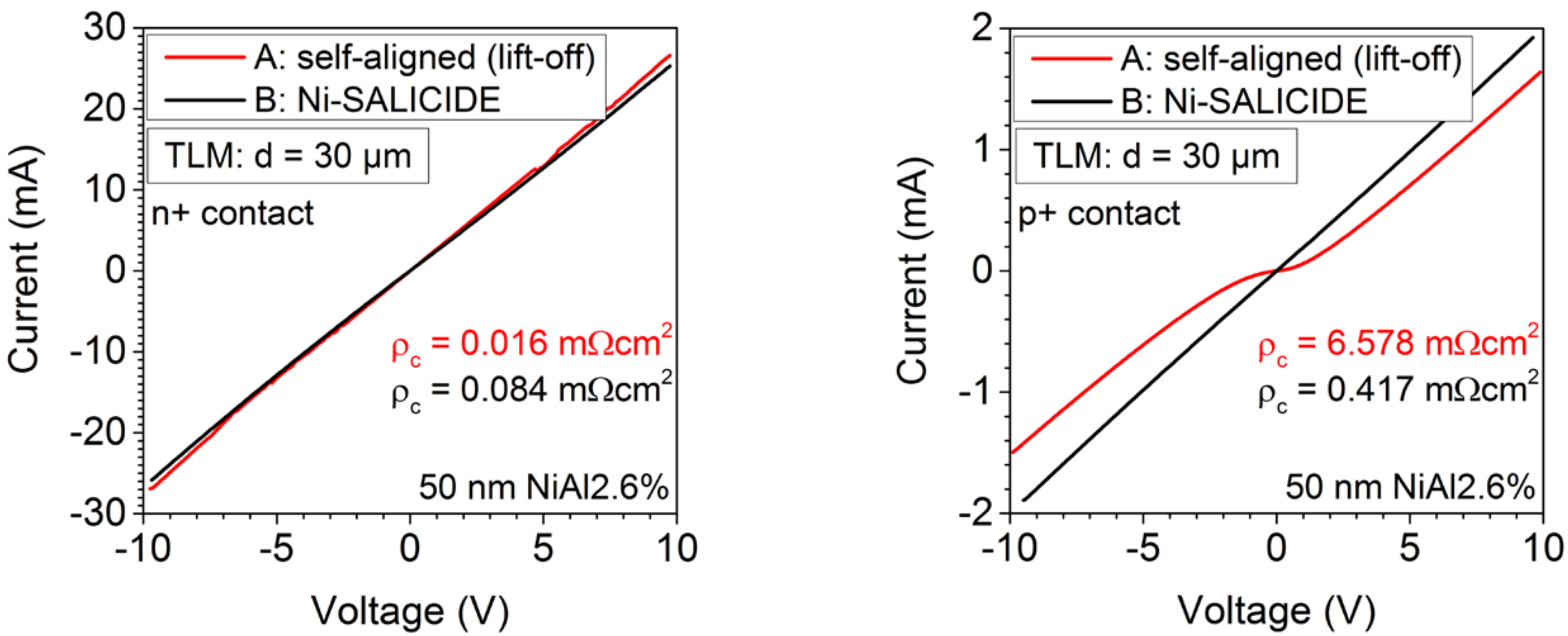
- Self-aligned and “Ni-SALICIDE” fabrication technologies
  - Comparison of fabrication technologies
    - Based on process developed at KTH



Ohmic contact formation

- Self-aligned and “Ni-SALICIDE” fabrication technologies
  - Comparison of fabrication technologies
    - Evaluation using TLM test patterns

Sledziewski et al., ECSCRM 2018



  - Both fabrication technologies are applicable depending on requirements

Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

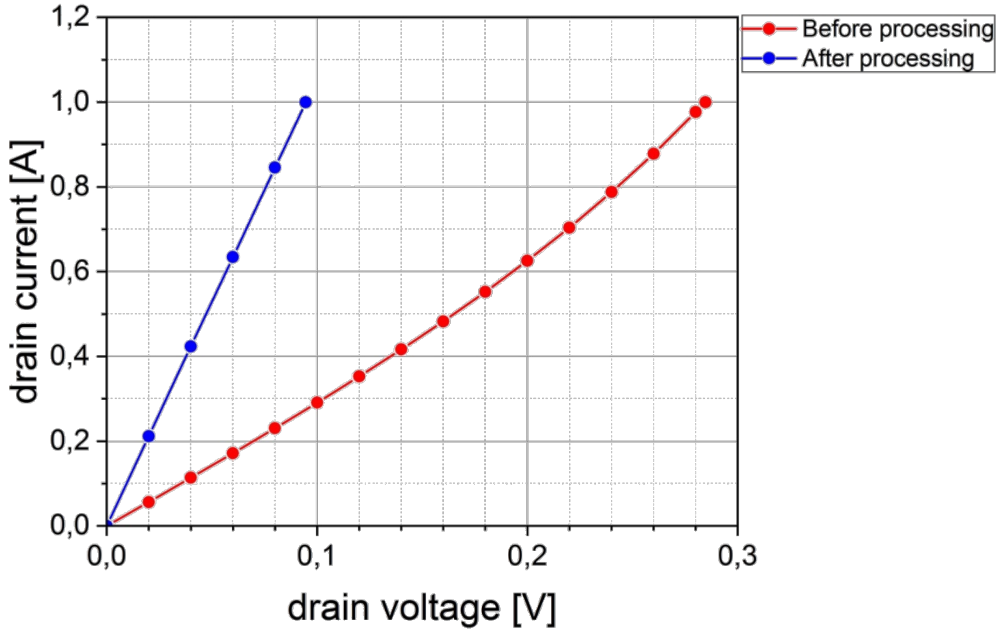
Device fabrication results

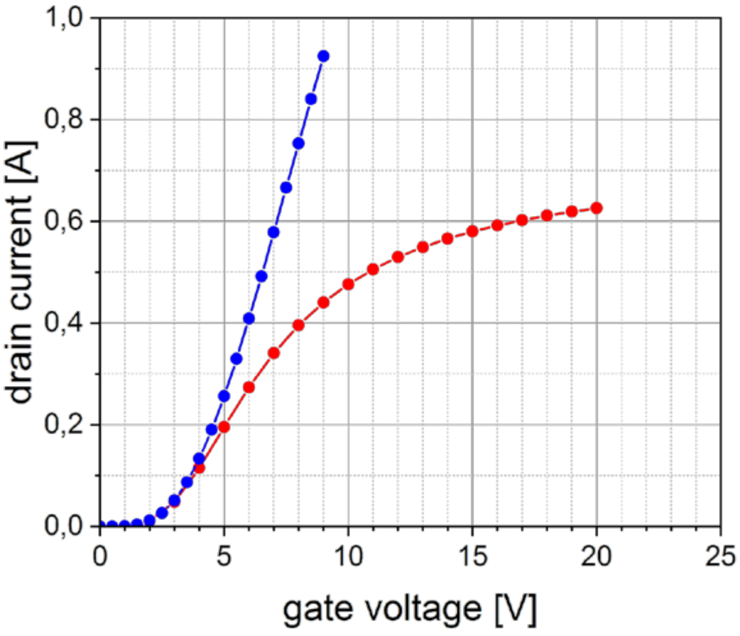
- Improvements of design, modelling and fabrication technologies allow for realization of competitive SiC power devices, e.g. 900V voltage class

  Breakdown voltage > 1100V — On-resistance < 100mΩ (9mΩcm^2)

  Threshold voltage: 1.6V — Yield > 40% @ 10mm^2

GRDC Project 2018





Device fabrication results

- Improvements of design, modelling and fabrication technologies allow for realization of competitive SiC power devices

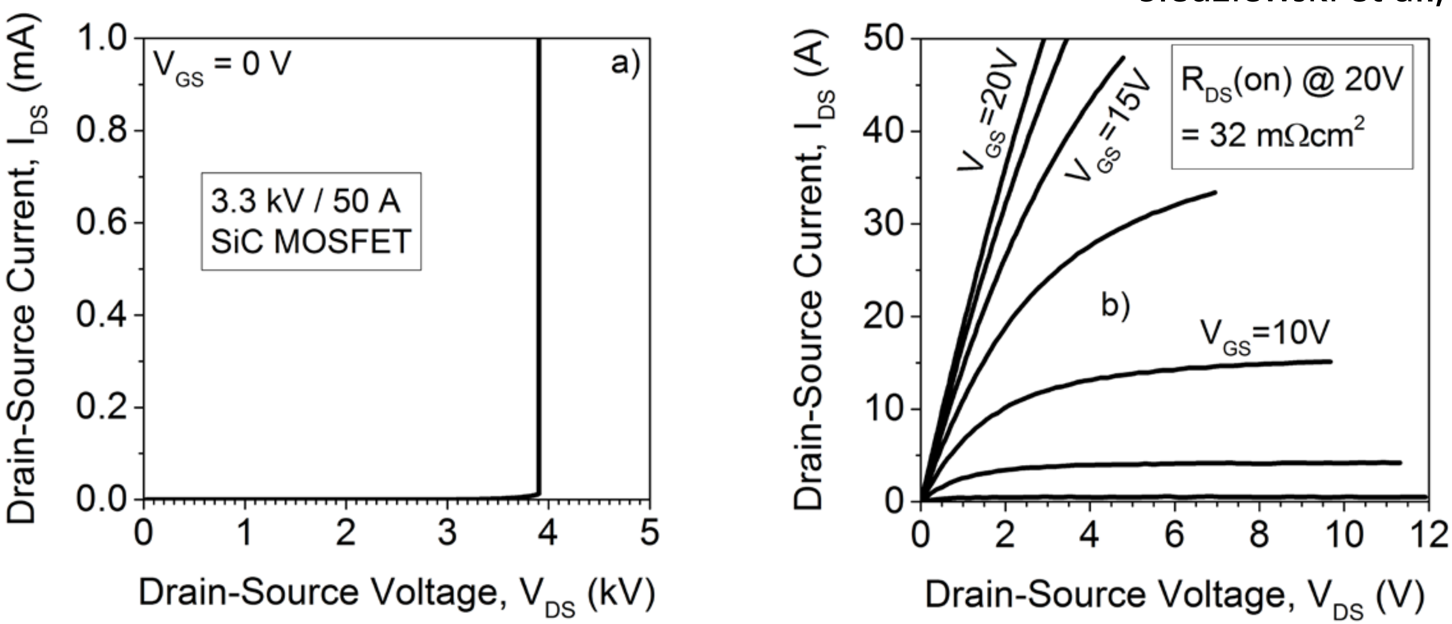
  Breakdown voltage > 3800V

  On-resistance: 32mΩcm²

  Threshold voltage: 3.0V

  Yield > 10% (Epitaxy defects)

Sledziewski et al., ECSCRM 2018



Content

- Motivation: Application pull and requirements for successful device design

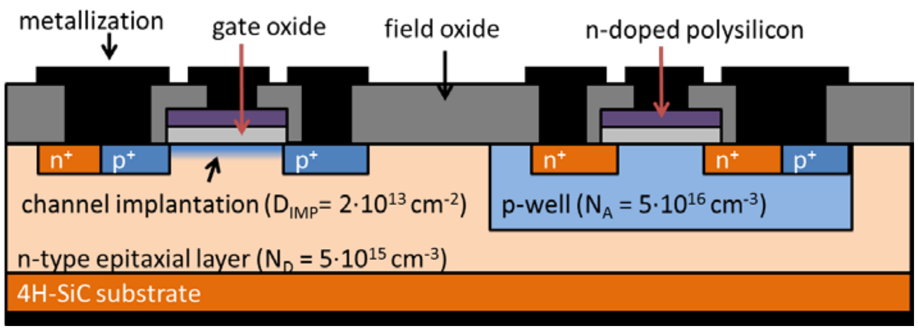
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits

- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices

- Conclusion

High temperature electronics beyond Silicon

- SiC MOS devices can be operated beyond 300°C
  - Development of SiC Power MOSFET technology allows for CMOS circuits
    - Silicon development went the other way!



  - High temperature circuits using "SiC power technology"
    - High temperature sensing
    - Signal amplification and conditioning
  - Challenge: Optimization of pMOS transistors

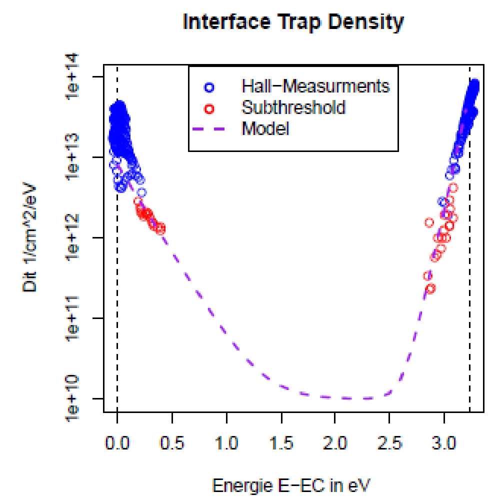
High temperature electronics beyond Silicon

- "Triple-well" SiC CMOS 1P1M technology
  - NMOS and PMOS transistors fabricated by ion implantation
  - Polygate process, 1Pt/Ti metal
  - Ohmic contact formation using NiAl and RTP
    - NMOS V_{Th}: 1.5V
    - PMOS V_{Th}: 7.0V, contact resistance!

→ There is still more work to do!

High temperature electronics beyond Silicon

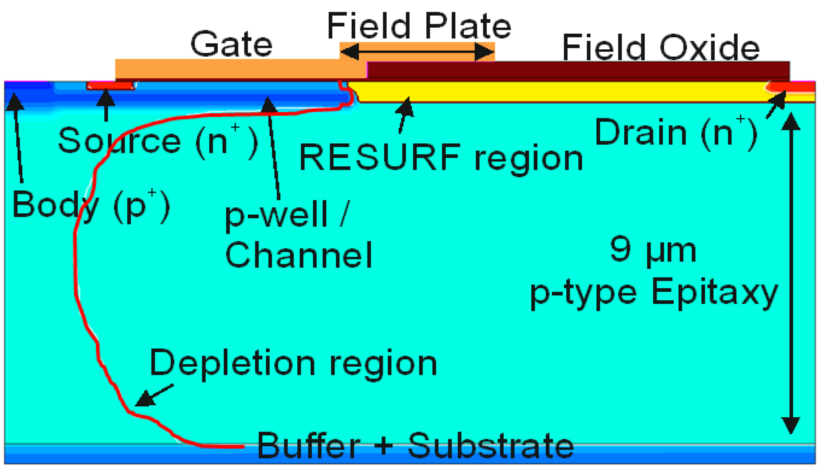
- Physical SPICE modelling for fast CMOS technology prototyping
  - Characterization of primitive devices (not IVs)
  - Extraction of physical and geometrical parameters
    - E.g. Interface state density, channel length
  - Modelling of device performance and comparison
  - SPICE Optimization:
    Fast BSIM model based on physical models



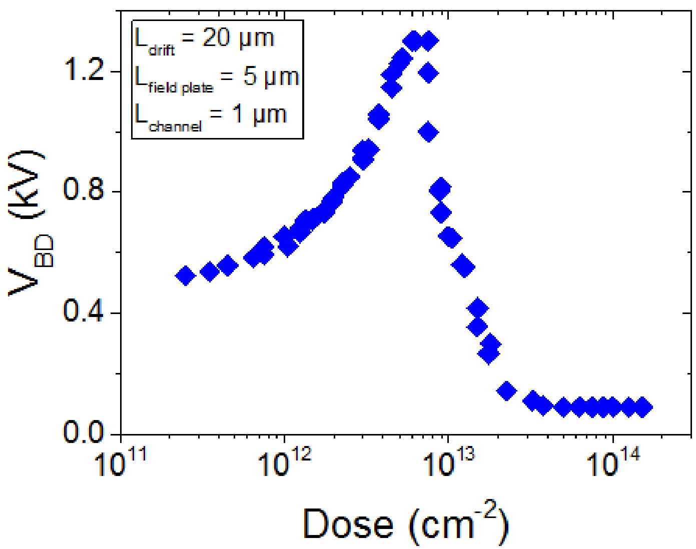
High voltage integrated circuits beyond Silicon

- Combination of CMOS and power device technology: Smart Power ICs
  - RESURF LDMOS: Another concept inspired from silicon technology

Weisse et al., ECSCRM 2018



Scheme of a lateral RESURF n-LDMOS transistor.



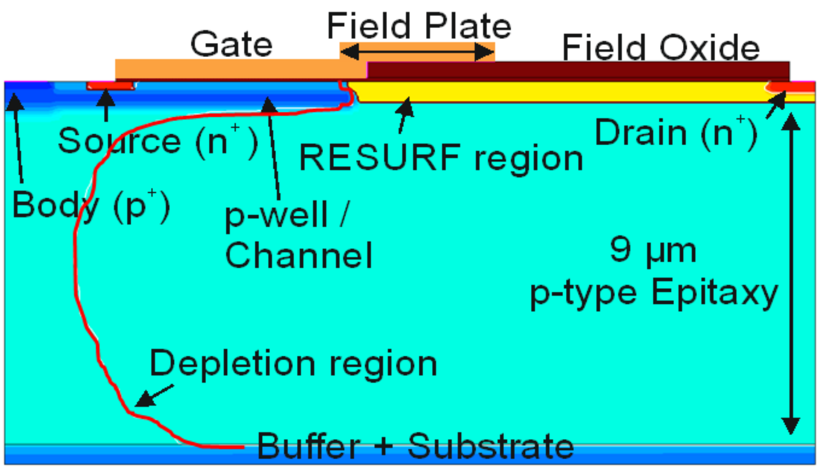
T. Erlbacher, 08.11.2018

Fraunhofer IISB

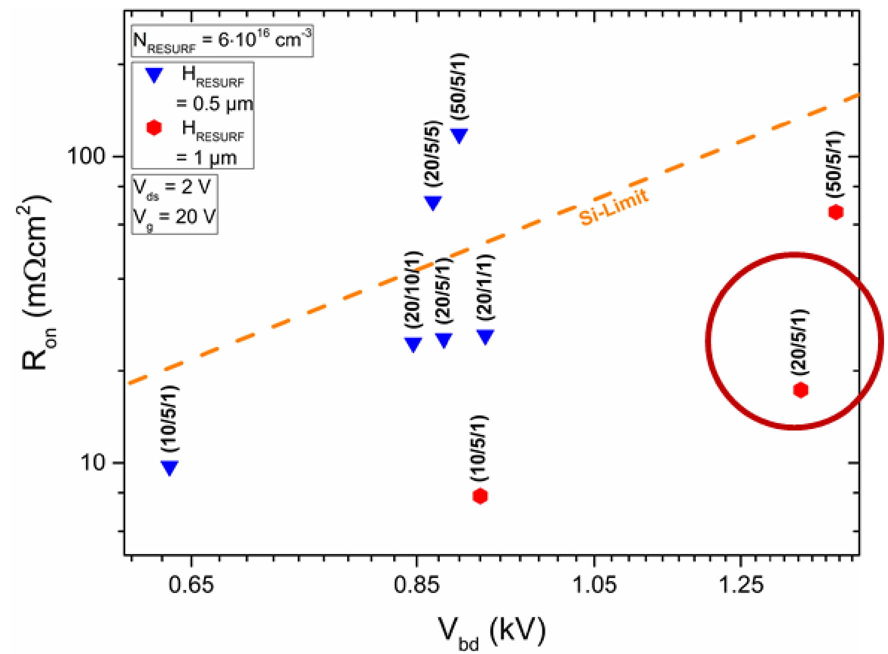
High voltage integrated circuits beyond Silicon

- Combination of CMOS and power device technology: Smart Power ICs
  - RESURF LDMOS: Another concept inspired from silicon technology

Weisse et al., ECSCRM 2018



Scheme of a lateral RESURF n-LDMOS transistor.



- 1200V SiC LDMOS will outperform silicon

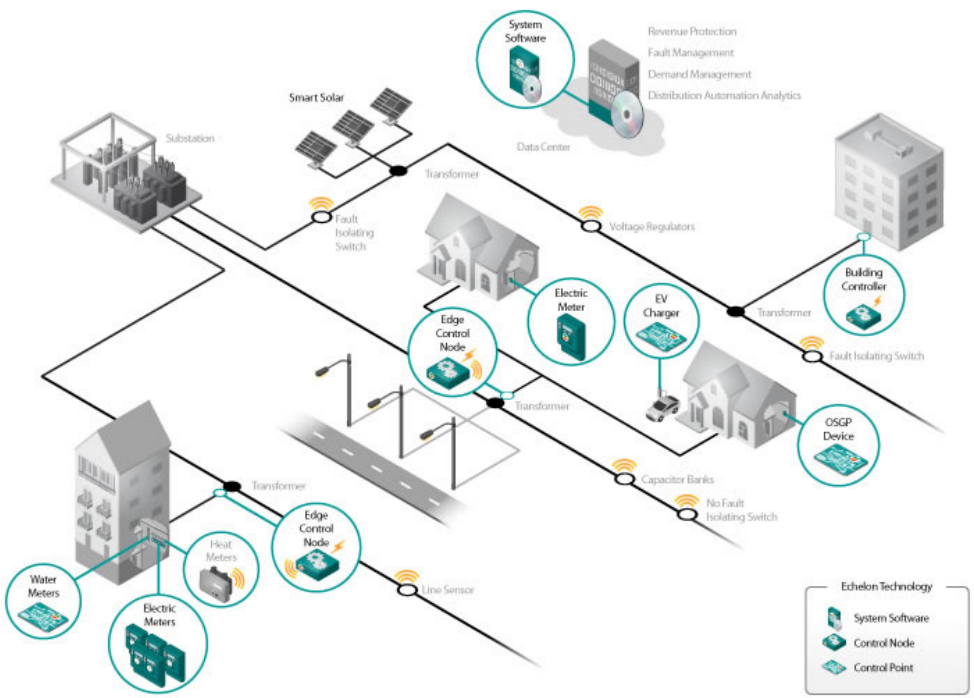
  → Charge balance is required (compare Al compensation)!

Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Solid state circuit breakers for DC grids

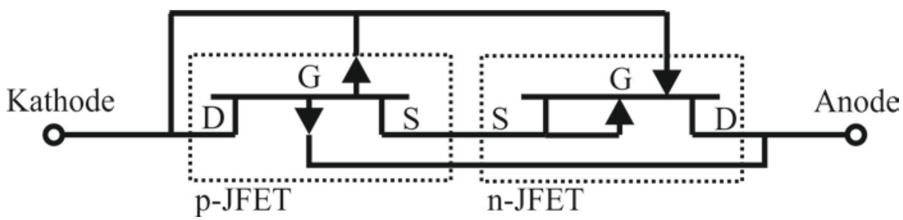
- Over-current protection in energy transmission grids
  - Circuit protection faster than mechanical breakers

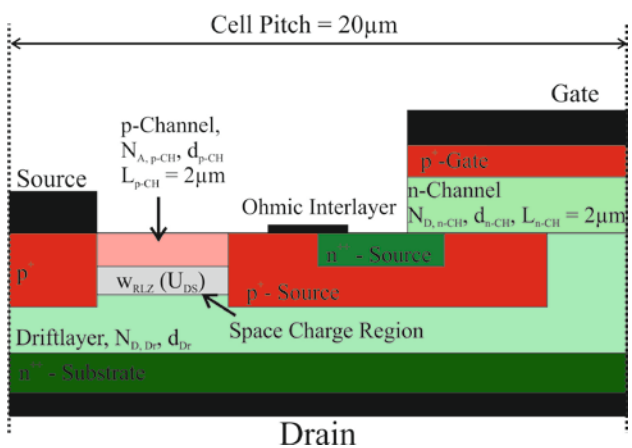


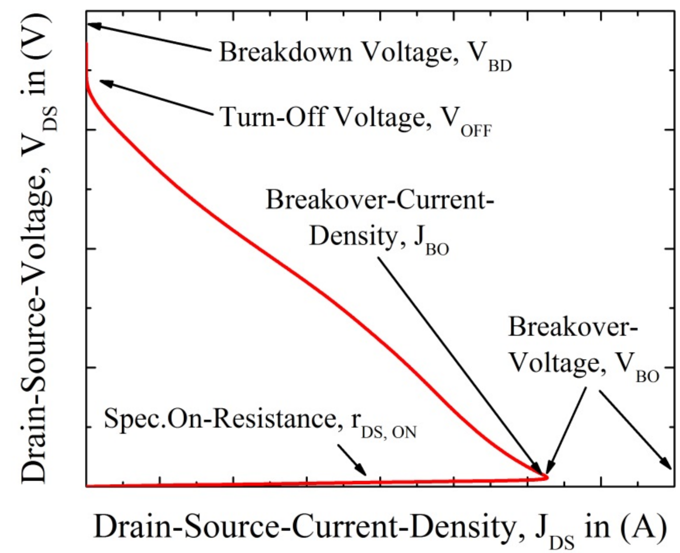
  - Robust and reliable solution desired

Solid state circuit breakers for DC grids

- Over-current protection in energy transmission grids
  - Normally-on device favorable (no external voltage bias required)
  - Monolithic integration (high integration density): Thyristor-dual
  - Self-triggering solution (fail-safe)







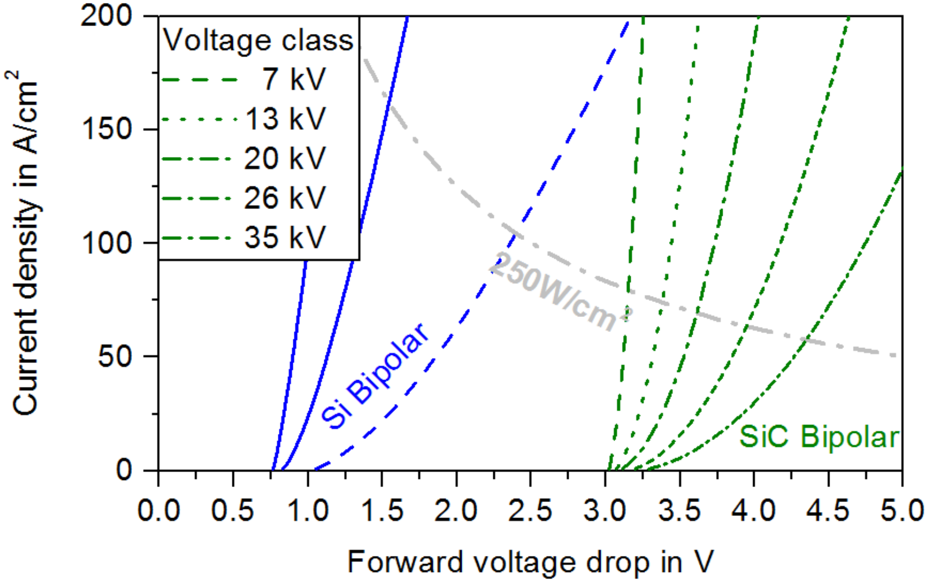
Huerner et al., ECSCRM 2016

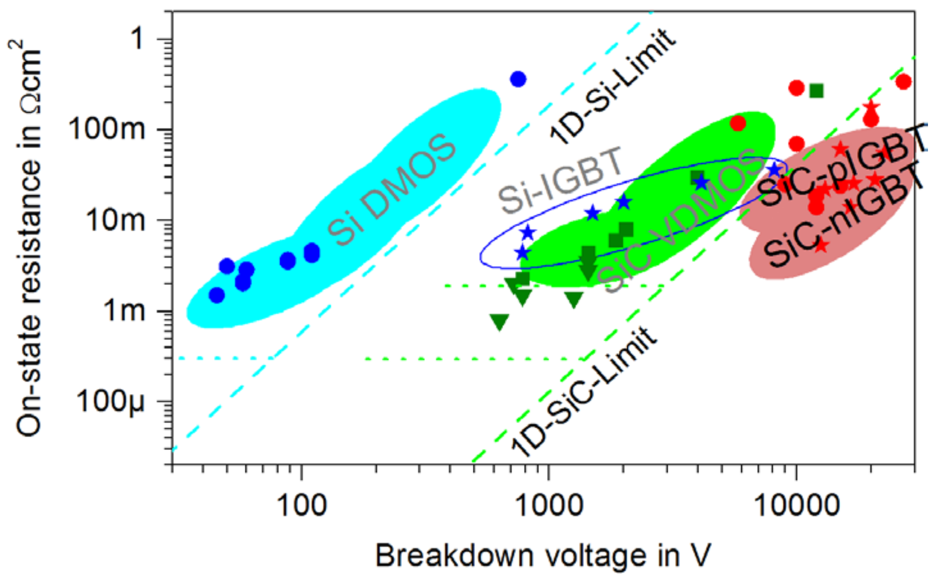
Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Insulated Gate Bipolar transistors

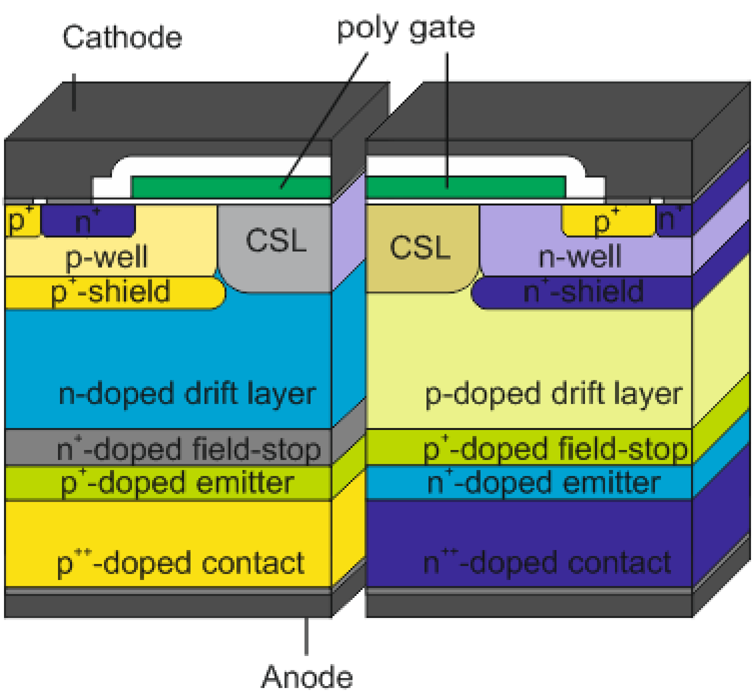
- Benefit of lower static losses 10kV+ SiC bipolar devices
  - Diffusion voltage in 4H-SiC: ≈ 3V → No direct competition to Si IGBTs
    - But high voltage power switches suitable for “Beyond Silicon”
      - Reduction of circuit complexity (see multi-level converters)
  - Challenge: Minority carrier lifetime!





Substrate technology: p- and n-doped drift regions

- Low resistance and high quality of available n^+-substrates
  - Development of p-IGBTs is "straight-forward", but…
  - Low channel mobility in pMOS (n-well)
  - Higher defect density in p-doped SiC
  - → Weaker conductivity modulation using p-IGBT
  - Lightly doped p-epitaxy layers are difficult to grow (background doping)

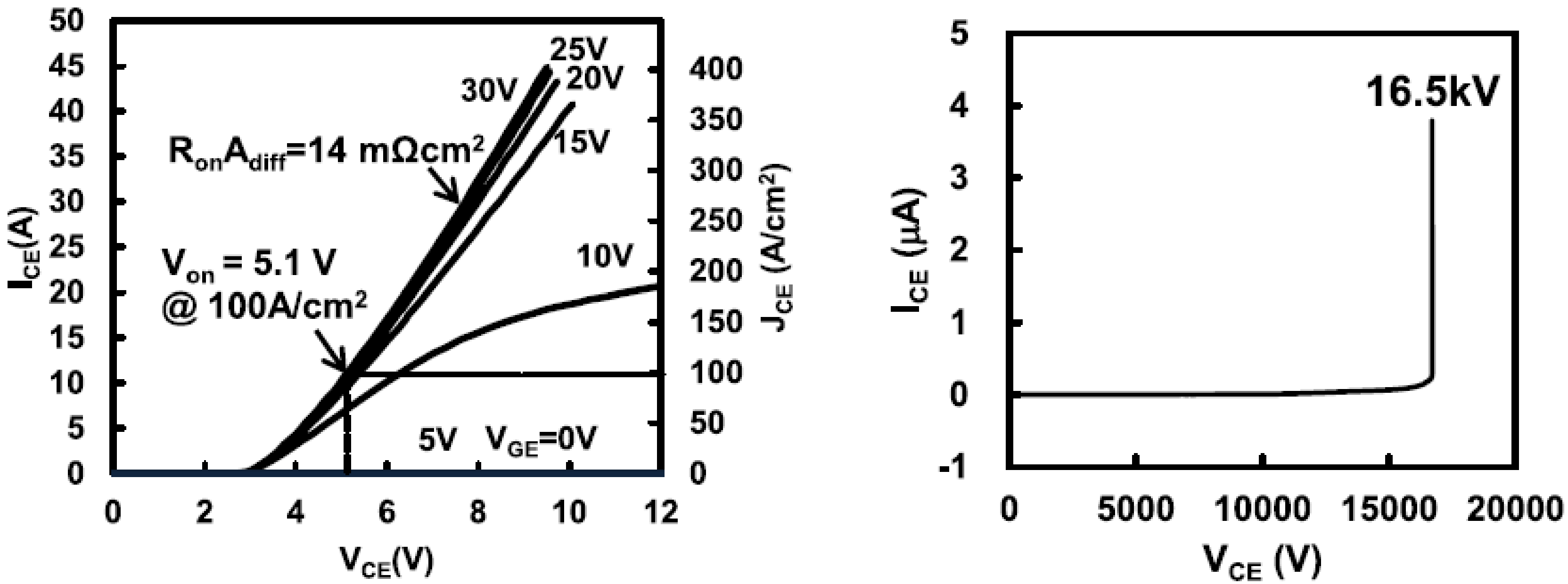


- Implementation of n-IGBT suffers from lack of availability of mature p^+-substrates and high substrate resistance
  - How to solve p^+-substrate issue?

Insulated Gate Bipolar transistors

- State-of-the-art in n-IGBTs R&D: 15kV devices
  - Carrier lifetime in drift region: 10µs
  - Thickness of drift region: 150µm
  - Junction termination: 800µm wide
  - Promising forward and blocking properties

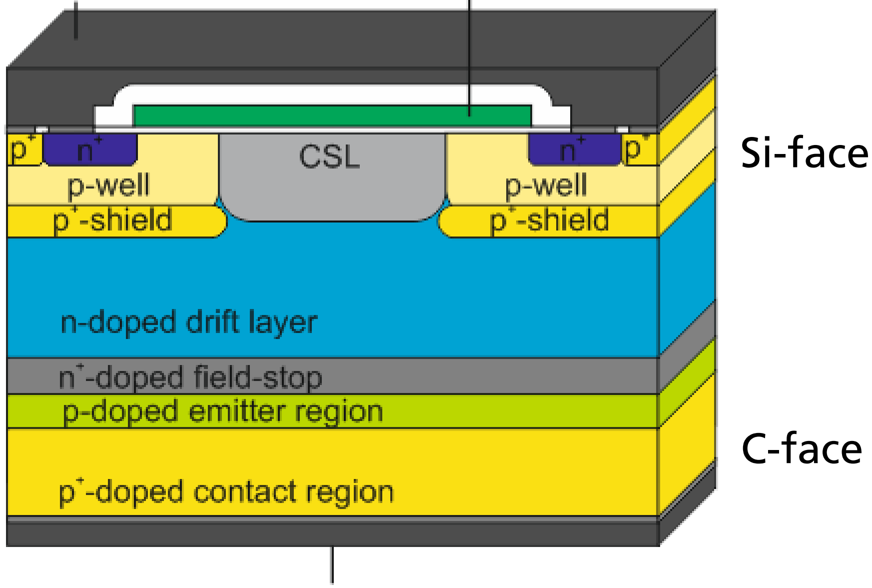
Fukada et al.,
Trans. Electron Dev. 62 (2015)



Fraunhofer
IISB

Substrate technology: p- and n-doped drift regions

- Device preparation of n-doped SiC with p-emitter
  - Backgrinding (Si-Side MOS)



Erlbacher et al., ICAE 2017

Example: Etched 100m wafer w/ Taiko ring (IISB)

  - Advantage: Use “standard” DMOS processing technology/sequencing

Content

- Motivation: Application pull and requirements for successful device design
- From modelling and design to device fabrication
  - Aluminum doping by ion implantation: Channeling and compensation
  - Ohmic contact formation on n^+ and p^+ contacts
  - Device fabrication results for VDMOS transistors and CMOS circuits
- SiC device concepts for future electronics using ion-implantation
  - High temperature electronics beyond silicon
  - Solid state circuit breakers for DC grids
  - Bipolar SiC devices
- Conclusion

Conclusion

- SiC technology is matured and physical understanding is fostered
  - Modelling is catching up → Reduction of development effort
  - Additional investigations into carrier lifetime improvement desirable
- SiC technology established – implementation of silicon device concepts
  - CMOS, IGBTs – generally: Concepts valid in Silicon technology
- SiC Bipolar devices are feasible for energy conversion applications
  - SiC IGBT in multi-level converter topologies (solid state transformer)
  - Medium voltage grid circuit breakers
- Reduction of semiconductor area (CAPEX) and power losses (OPEX) possible

  → Innovation!

Prototype fabrication at Fraunhofer IISB: Access to P-Fab

- 150mm SiC pilot line
  - Based on 200mm silicon CMOS line
  - Fabrication of SiC-devices qualified (ISO 9001) processing environment

π-Fab®

qualityaustria
SYSTEM CERTIFIED
ISO 9001:2008 No.16300/0

Thank you for Your attention!

The work shown was supported by

- The Korean NRF under the Global Research Development Center (GRDC) in the POSTECH-Fraunhofer IISB Joint Research
- The German Research Foundation (DFG, project ER755/1-1)
- The European Commission under grant number 604075 (SPEED)