IMPROVED EMITTERS BY DRY ETCHING

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ABSTRACT: A selective emitter by means of lowly doped regions with a low saturation current between the contact fingers and highly doped regions below the fingers can significantly improve the cell efficiency of crystalline silicon solar cells. A low saturation current could be achieved for diffused emitters by etching back the surface layer containing the high concentration of electrical inactive phosphorous ("dead-layer"). The significant benefit of performing this etch-process with plasma is the possibility to include it in one vacuum chamber with a subsequent anti-reflection coating (ARC). In this work a homogeneous etch-back of the emitter by means of SF_6-plasma-etching is presented. The passivation quality of a silicon nitride ARC and of a silicon-rich silicon oxynitride / silicon nitride double layer ARC deposited on plasma-etched emitters is investigated. Emitter saturation currents down to J_{0e} = 57 fA/cm^2 are achieved.

Keywords: dry-etching, PECVD, passivation, selective emitter, silicon nitride

1 INTRODUCTION

Selective emitter structures can significantly improve the blue response and the open-circuit voltage of crystalline silicon solar cells. To achieve this structure several approaches were released in the last years [1-4]. A low emitter saturation current J_{0e} could be achieved for a diffused emitter by etching back the surface layer containing a high electrically inactive phosphorous concentration (dead-layer). Haverkamp *et al.* have shown that by masking the contact regions on a diffused emitter and etching back the high phosphorous surface concentration between the fingers a functional selective emitter structure could be achieved [4]. By using a laser doping out of the phosphosilicate glass (PSG) as described by Jäger *et al.* phosphorous is driven in deeply into the silicon substrate ($N_D > 10^{20}$ cm^{-3} for over 200 nm) in the contact areas [5]. In addition to a masking-free full-surface etch-back of about 50 nm the emitter between the contacts could be significantly improved while maintaining a high doping level in the laser processed area. Therefore the aimed selective emitter structure could be achieved as sketched in Figure 1 by only adding two simple process steps to a standard production scheme:

1) Laser doping from PSG.

2) Homogeneous full surface etch-back by plasma etching before the silicon-nitride deposition in the same vacuum tool.

In this work, the dry-etching process will be developed for this purpose. Dry-etching processes for crystalline silicon solar cells have been proposed for several years [6-8]. But up to now, these processes are mostly developed to replace the wet chemical etching processes as texturing, polishing or PSG-removal and for these purposes too low etch rates prevent a wide-spread application in industrial production so far. In this work a new task for plasma-etching processes is introduced, where the low etch-rate could be exploited for a very small but homogeneous surface etch-back. For this process not the etch rate is the focus, but the homogeneity and the quality of a surface passivation layer deposited subsequently in one vacuum step.

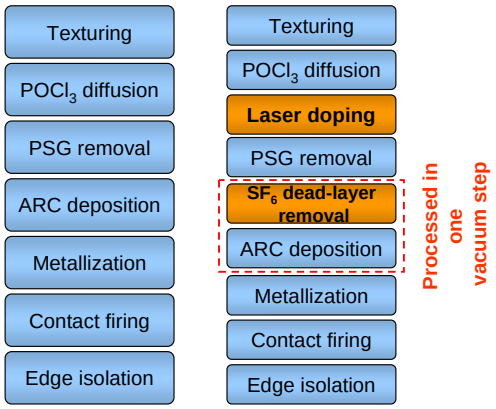

Figure 1: Possible process series to achieve a selective emitter structure by adding only two process steps to a standard cell production process.

Besides the application for a selective emitter, the SF_6 dead-layer removal can be used to improve an emitter with a shorter etch step, so that the phosphorous concentration is still high enough for screen-printed contacts. Such an application is used in [9].

2 EXPERIMENTAL

The plasma etching with subsequent ARC deposition has been performed at a modified semi-inline SiNA system by Roth&Rau, which provides etching- and deposition-sources within one vacuum chamber. The plasma is excited by a 2.45 GHz microwave coupled in by a linear

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copper antenna over a width of 0.9 m.

Two materials have been used as substrate during this work:

- Boron-doped Cz-silicon wafers (ρ = 1-3 Ω cm; 125×125 mm^2 pseudosquare) with a random-pyramids-textured surface.
- Boron-doped FZ-silicon wafers (ρ = 1 Ω cm, 60×60 mm^2) with a shiny-etched surface.

All wafers received a $POCl_3$-diffused emitter with sheet resistance R_{sh} = 60 Ω/sq, grown in a tube furnace. The phosphosilicate glass (PSG) is removed in diluted hydrofluoric acid (HF). The samples were etched in sulphur hexafluoride (SF_6) plasma for about 5 s to remove the dead layer containing the high electrically inactive phosphorous concentration. Subsequently, the ARC is deposited without an additional cleaning or after two different plasma-cleaning processes:

- An ammonia (NH_3)-plasma cleaning for about 12 s in pure NH_3 plasma. Such a cleaning has already shown a beneficial effect in previous work [8].
- A SF_6-plasma cleaning for about 12 s, which in contrast to the previous SF_6 etching is performed at such a high process pressure that the ion energies are low enough to inhibit a significant silicon removal. No detectable change in R_{sh} occurs with this process.

As the plasma-etching, -cleaning and -deposition processes were performed in the same vacuum chamber, all processes had to be performed at one temperature ($T_{process}$ = 350°C).

For reference, one sample is only passivated after PSG removal without any dead-layer etching. Two different surface passivation layers are compared on the samples. A standard amorphous hydrogenated silicon nitride (a-SiN_x:H) as commonly used as ARC for silicon solar cells and a double-layer of amorphous hydrogen- and silicon-rich silicon oxynitride (SiriON) and a-SiN_x:H, which can result in an improved surface passivation, while maintaining a good ARC ability [10]. Finally, the wafers have received a fast-firing step at 820°C in a belt furnace. The process-sequence is sketched in Figure 2.

All samples are treated symmetrically on both surfaces to allow effective charge carrier lifetime(τ_{eff}) measurements using a standard quasi-steady-state photoconductance (QSSPC) measurement tool (Sinton, WCT-100). Additionally one textured Cz wafer has been used without ARC to monitor the etch homogeneity of the dead-layer removal by a spatially resolved R_{sh}-measurement using a four-point-probe measurement tool.

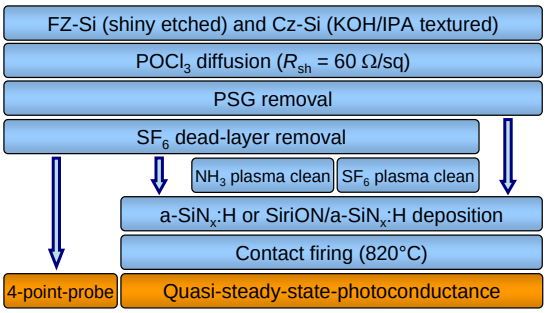

Figure 2: Process-sequence for the investigated samples; all wafers are treated symmetrically on both surfaces.

3 RESULTS

As can be seen in Figure 3, the emitter sheet resistance has been increased for the textured Cz wafers by the SF_6-etch process in average to 107 Ω/sq. A very good homogeneity has been achieved with a standard deviation of 3 Ω/sq over the whole wafer. Due to the smaller surface the shiny-etched FZ wafers are etched faster in plasma. As they have been processed in parallel to the textured wafers the resulting sheet resistance was R_{sh} = 141 Ω/sq. This value is too high for an effective selective emitter using screen printed contact fingers, but good to investigate the quality of a subsequently deposited surface passivation.

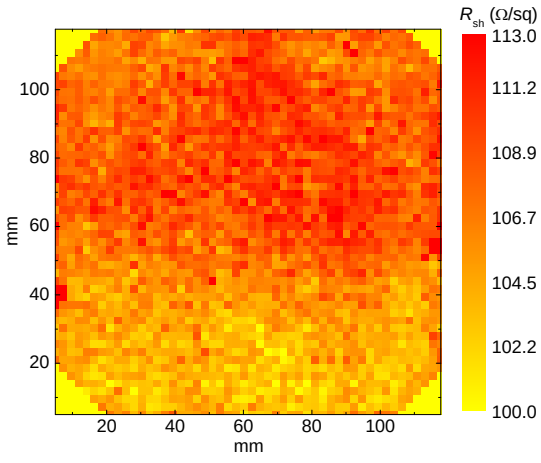

Figure 3: Sheet resistance map of a textured SF_6-etched wafer with an originally diffused emitter of R_{sh} = 60 Ω/sq. The emitter is homogeneously etched back to R_{sh} = 107 Ω/sq with a standard deviation of 3 Ω/sq.

In Figure 4 the effective charge carrier lifetimes τ_{eff} of the shiny-etched FZ wafers are plotted after deposition and after a contact-firing step at 820°C. Additionally, the emitter saturation current J_{0e} is calculated via [11]:

$$J_{0e} = \frac{qn_i^2 W}{2(N_{dop} + \Delta n)} \left\{ \frac{1}{\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}} - \frac{1}{D_{min}} \left(\frac{W}{\pi} \right)^2 \right\}^{-1} \qquad (1)$$

with the intrinsic carrier density $n_i = 9.143 \times 10^9$ cm^{-3} [12], the elementary charge q, the minority diffusion constant D_{min}, the doping concentration N_{dop}, the minority excess charge carrier density Δn and the wafer thickness W. The bulk lifetime τ_{bulk} has been calculated using the Auger-recombination model of Kerr and Cuevas [13].

It is noticeable that the charge carrier recombination is reduced for all processes with etched emitters compared to the original emitter. This indicates the emitter improvement by the dead-layer removal. The direct ARC deposition in the vacuum chamber after the etching seems to be problematic for the pure a-SiN$_x$:H passivation. Here only an emitter saturation current of $J_{0e} = 159$ fA/cm^2 is reached after the firing step. The deposited a-SiN$_x$:H performs better after an additional plasma-cleaning step. The best surface passivation is achieved for the sample with the additional NH$_3$-preconditioning ($J_{0e} = 77$ fA/cm^2). The preconditioning with a non-etching SF$_6$ plasma results in a quite similar improvement after firing: $J_{0e} = 97$ fA/cm^2.

Surface passivation with the SiriON/a-SiN$_x$:H double layer seems to be less sensitive to the plasma-etched surface. With this layer-system the deposition directly after the SF$_6$-etch-process leads already to an effective surface passivation quality after the firing step of $J_{0e} = 82$ fA/cm^2. However the two plasma-cleaning processes further improve the surface passivation quality, resulting in $J_{0e} = 72$ fA/cm^2 after the NH$_3$-plasma and $J_{0e} = 57$ fA/cm^2 after SF$_6$-plasma cleaning. It is remarked that this layer stack is also adapted as ARC as is described in [10].

For the Cz wafers the picture is quite similar, as can be seen in Figure 5. As the material is degraded by 18 h illumination after the firing step the bulk lifetime is comparably low and it makes no sense to calculate the emitter saturation current for these samples using an only-Auger-limited τ_{bulk}. The trends, which have been observed before for the FZ samples, were reproduced for the textured Cz wafers. The poor surface passivation of the a-SiN$_x$:H layer by depositing directly after the emitter-etching is even more evident. For the samples including an additional SF$_6$-plasma cleaning and for the SiriON/a-SiN$_x$:H layer deposited without a further cleaning step after the etch process effective lifetimes around 50 µs are reached. Including a NH$_3$-plasma cleaning even 60 µs are reached, which is expected to be in the range of the bulk lifetime of this material in the degraded state.

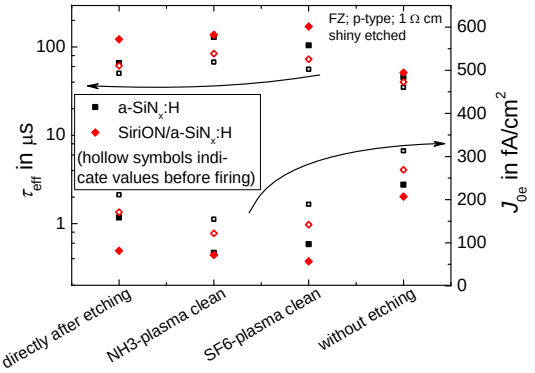

Figure 4: Effective charge carrier lifetime τ_{eff} at $\Delta n = 10^{15}$ cm^{-3} and the emitter saturation current density J_{0e} calculated after eq.(1) for the FZ wafers with the diffused emitter etched back with SF$_6$ plasma to $R_{sh} = 141$ Ω/sq. τ_{eff} is compared for samples passivated directly after the etch process, samples with an NH$_3$ plasma cleaning or a SF$_6$ plasma cleaning between etching and passivation and as reference for samples without an emitter etching passivated after the PSG removal. For all processes one sample was passivated with a standard a-SiN$_x$:H and one sample with a SiriON/a-SiN$_x$:H double layer, which were measured after deposition (hollow symbols) and after a contact-firing step at 820 °C (solid symbols).

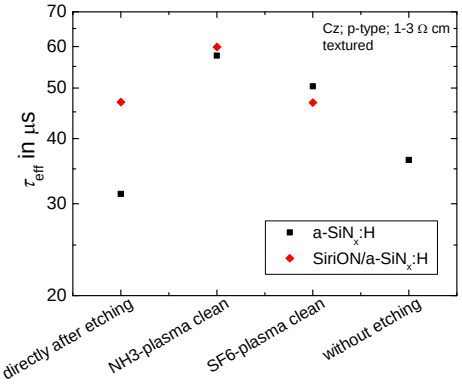

Figure 5: Effective charge carrier lifetime τ_{eff} at $\Delta n = 10^{15}$ cm^{-3} for the textured Cz-wafers with the emitter etched back to $R_{sh} = 107$ Ω/sq. The wafers are measured after a contact firing step at 820°C and degradation (18h illumination).

4 SUMMARY

In this work a dead-layer removal by means of a SF$_6$-plasma-etch process has been successfully introduced. It has been demonstrated that a homogeneous lift in the sheet resistance from $R_{sh} = 60$ Ω/sq to $R_{sh} = (107 \pm 3)$ Ω/sq is possible by a ca. 5 s long process in an industrial-type inline plasma tool. Furthermore, the surface passivation qualities of two subsequently deposited AR coatings (a standard a-SiN$_x$:H ARC and a

SiriON/a-SiN_x:H AR-double-layer coating) has been investigated. It has been observed, that the SiriON/a-SiN_x:H double layer performs better than the a-SiN_x:H layer on the plasma-etched surface. Especially the latter can benefit from an additionally NH_3-plasma cleaning or from a SF_6-plasma cleaning after the etching. On shiny-etched FZ silicon with an emitter etched back to R_{sh} = 141 Ω/sq an emitter saturation current of J_{0e} = 57 fA/cm^2 was presented. On alkalinely textured Cz wafers the emitter was etched to R_{sh} = 107 Ω/sq and effective charge carrier lifetimes up to 60 µs were reached after degradation. This demonstrates that the process is suitable for an industrial high-efficiency selective-emitter realization.

5 ACKNOWLEDGMENTS

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