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4.5 kV SiC Junction Barrier Schottky Diodes with Low Leakage Current and High Forward Current Density

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Motivation

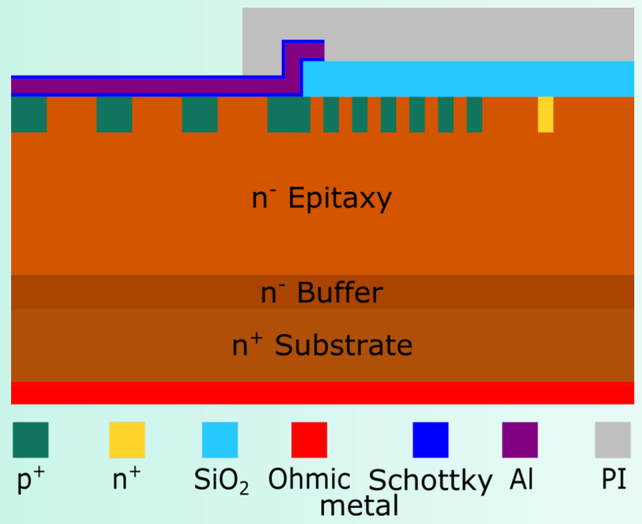
- SiC diodes with high blocking voltage as well as high current carrying capability not yet available on the market
- Junction Barrier Schottky (JBS) design to profit from lower leakage current at still high forward current [1, 2]
- Fabrication in Si CMOS line upgraded to SiC capability offers economical process

Fabrication

- Alignment mark etching and deposition of scattering oxide
- p^+ front side implantation to form JBS pattern and field rings
- n^+ front side implantation to form channel stopper ring
- n^+ back side implantation to enhance ohmic contact formation
- High-temperature anneal to activate dopants with carbon cap
- Thermal oxide growth and deposition of oxide as passivation outside of the active diode area
- Back side ohmic contact formed by alloying NiAl (2.6%) via Rapid Thermal Processing (RTP) in graphite box
- Formation of Schottky top contact with sputtered titanium, covered by aluminum
- Reinforcement of back side contact with thick aluminum layer
- Tempering of Schottky metal with forming gas anneal
- Polyimide passivation and solderable back side metal stack added
- Bonded and soldered diced chips onto DBC substrates for high current measurements

Design

- Epitaxy: 4H-SiC, 32 µm, N-doped 1 x 10^{15} cm^{-3}, production grade quality
- Junction barrier formed by p^+ implant (4 µm width, 4 µm spacing)
- Edge termination using Floating Field Rings (FFR) formed by p^+ implant (10 µm width, spacing increasing from 2 to 5 µm, 36 rings) and n^+ channel stopper in favor of Junction Termination Extension (JTE) to allow greater processing tolerance [3]
- Die size 7 mm x 7 mm, active area 0.25 cm^2

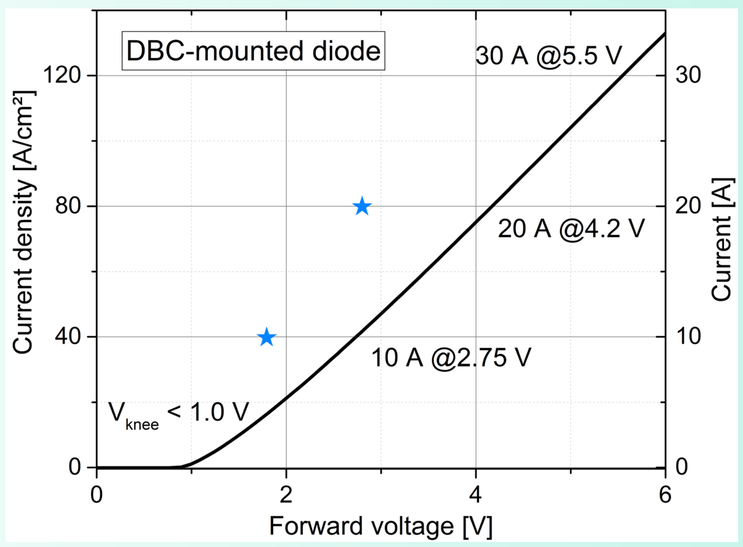


Implant	Total dose	Max. energy	Box profile depth
p+	2.65 x 10^{14} cm^{-2}	400 keV	500 nm
n+ channel stopper	1.0 x 10^{15} cm^{-2}	120 keV	500 nm
n+ back side contact	4.2 x 10^{14} cm^{-2}	65 keV	100 nm

Electrical Characterization

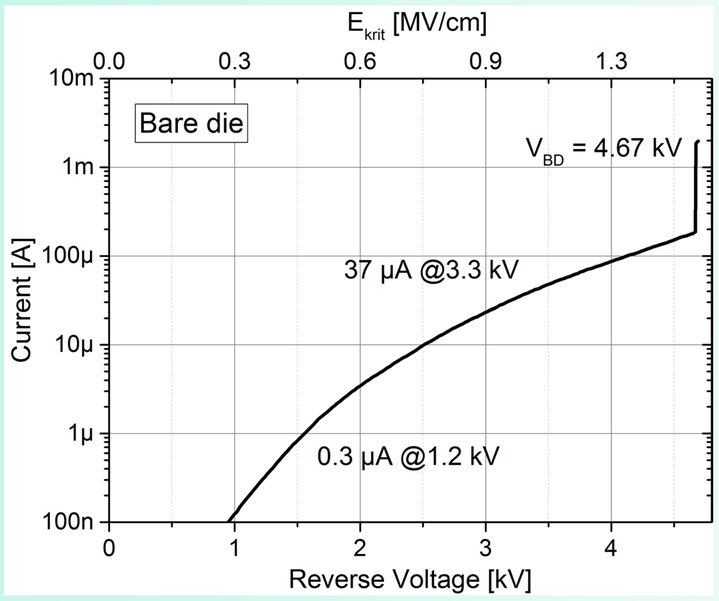
Forward IV

- Diodes turn-on below 1 V
- Schottky barrier ϕ_B = 1.2 V and ideality factor n = 1.07
- High current pulsed measurement with bonded and DBC-mounted diodes
- Current density of over 100 A/cm^2 at 5 V
- No degradation observed at current density of over 300 A/cm^2 at 15 V
- Presented epitaxial parameters were chosen to withstand high voltage
- Optimized parameters may result in up to 100 mΩ cm lower resistivity and nearly 1 V lower voltage drop at 10 A (see stars in plot) at identical breakdown voltage



Reverse IV

- Bare die measured at room temperature with inert liquid as additional passivation
- Breakdown occurred at voltages over 4.6 kV (73 % of theoretical maximum value)
- Leakage currents were low with 300 nA at 1.2 kV and 37 µA at 3.3 kV, demonstrating the effectivity of the applied JBS-design
- Non-destructive breakdown at current compliance of 10 mA



Summary and Outlook

- Fabrication of high performing SiC diodes in an upgraded Si CMOS line was demonstrated
- Diodes feature a breakdown voltage of over 4.5 kV
- Current carrying capability of 10 A was realized at a voltage drop of 2.75 V
- Current density of over 300 A/cm^2 was reached without degradation
- Substrate with optimized drift layer thickness and doping will result in up to 100 mΩ cm lower resistivity at identical breakdown voltage

	Drift layer doping	Drift layer width	Voltage drop at 10 A
Presented work	1 x 10^{15} cm^{-3}	32 µm	2.75 V
Optimized	2.75 x 10^{15} cm^{-3}	30 µm	1.8 V

Acknowledgment

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