FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB

International Conference on Silicon Carbide and Related Materials, September 29th – October 4th 2019, Kyoto, Japan

# Low-resistance ohmic contact formation by laser annealing of N-implanted 4H-SiC


C. Hellinger [1, a], O. Rusch [1, b], M. Rommel[1, c], A. J. Bauer [1, d], T. Erlbacher [1, 2, e]

*[1] Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany*
*[2] Chair of Electron Devices, University Erlangen-Nuremberg, Erlangen, Germany*
*[a] carsten.hellinger@iisb.fraunhofer.de, [b] oleg.rusch@iisb.fraunhofer.de, [c] mathias.rommel@iisb.fraunhofer.de, [d] anton.bauer@iisb.fraunhofer.de,*
*[e] tobias.erlbacher@iisb.fraunhofer.de*


## Motivation

- Minimizing power losses of vertical devices by manufacturing low-resistance ohmic contacts and reducing wafer thickness
- Creating low-resistance ohmic contacts by ion implantation and suitable metallization
- Usually post-implant annealing in a high temperature furnace (> 1500°C) necessary to recover lattice and electrically activate the dopants [1]
- Performing thinning step after finishing wafer frontside

→ No classic post-implant annealing possible

→ **Using a UV laser for post-implant annealing and ohmic contact formation**

## Laser annealing parameters

- Post-implant annealing parameters:

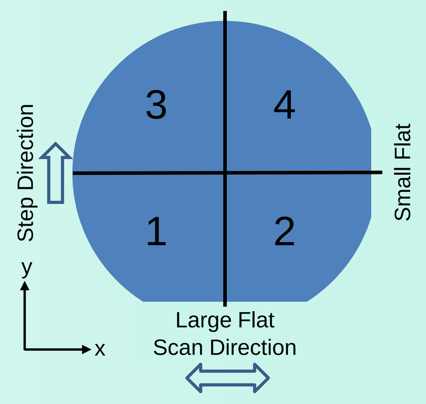
| quarter | number of repetitions | energy density [J/cm²] | | | overlap [%] | |
|---|---|---|---|---|---|---|
| | | 1st pass | 2nd pass | 3rd pass | scan | step |
| 1 | 1 | 1.7 | 2.5 | 3.0 | 75 | 75 |
| 2 | 1 | 3.0 | 3.0 | 3.0 | 85 | 75 |
| 3 | 3 | 1.7 | 2.5 | 3.0 | 75 | 75 |
| 4 | No post-implant annealing | | | | | |

Frequency tripled Nd:YVO$_4$ with 355 nm wavelength, 80 µm beamsize, 60 ns pulse duration

- Contact annealing parameters:

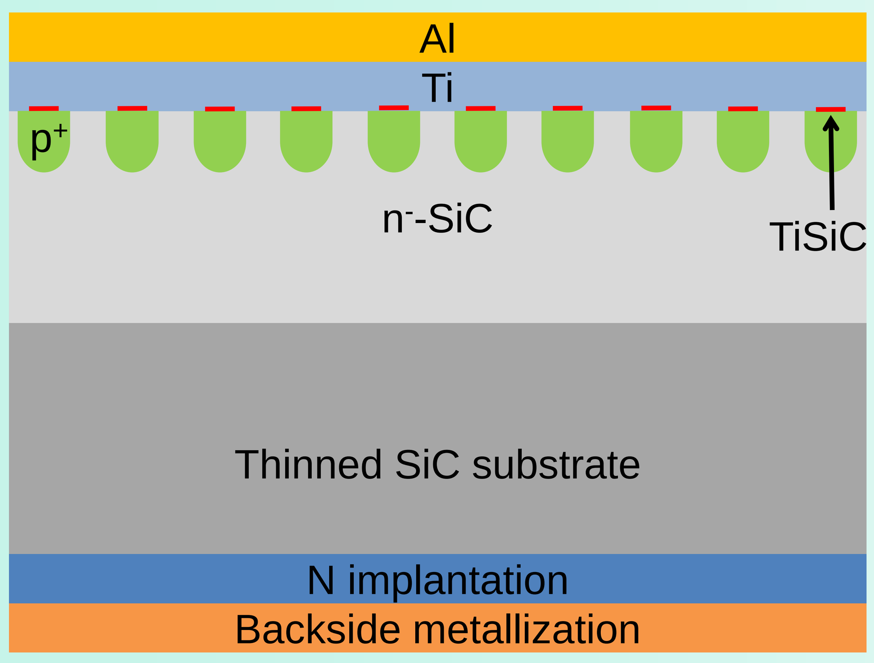
| quarter | energy density [J/cm²] | overlap [%] | |
|---|---|---|---|
| | | scan | step |
| 1 to 4 | 3.3 | 67 | 50 |

Frequency tripled Nd:YVO$_4$ with 355 nm wavelength, 80 µm beamsize, 48 ns pulse duration




## Fabrication

- Fabrication of vertical JBS diodes on commercial 100 mm 4H-SiC epitaxial wafers
- JBS pattern formed by p⁺ implantation
- JBS diodes with 4 different designs, differing in distance between and width of p⁺ stripes
- Metallization systems:
  - Schottky: titanium (Ti)
  - Ohmic: silicided Ti (TiSiC)
  - Power metallization: aluminum (Al)
- Temporary bonding of frontside finished device wafer to carrier wafer
- Backgrinding of device wafer to 120 µm
- N implantation on the wafer backside
- Post-implant annealing by laser
- Deposition of nickel as ohmic contact metal
- Forming ohmic contact by laser annealing
- Deposition of solderable stack
- Debonding of temporary bonded device wafer




Parameters of backside implantation

| energy [keV] | dose [1/cm²] |
|---|---|
| 90 | 4E14 |
| 50 | 2.3E14 |
| 25 | 2E14 |

## Results

- Sheet resistance in post-implant laser annealed quarters significantly lower than in not-annealed quarter, which is in usual range compared to standard process (fig. a)
- Specific resistance in not-annealed quarter after ohmic contact formation annealing still higher than in post-implant laser annealed quarters (fig. b)
- Voltage drop of 40 mV at 6 A for post-implant laser annealed JBS diodes compared to not-annealed quarter (fig. c)
- Forward voltage at 6 A depending on p⁺ stripe design, but voltage drop independent of the design (fig. d)

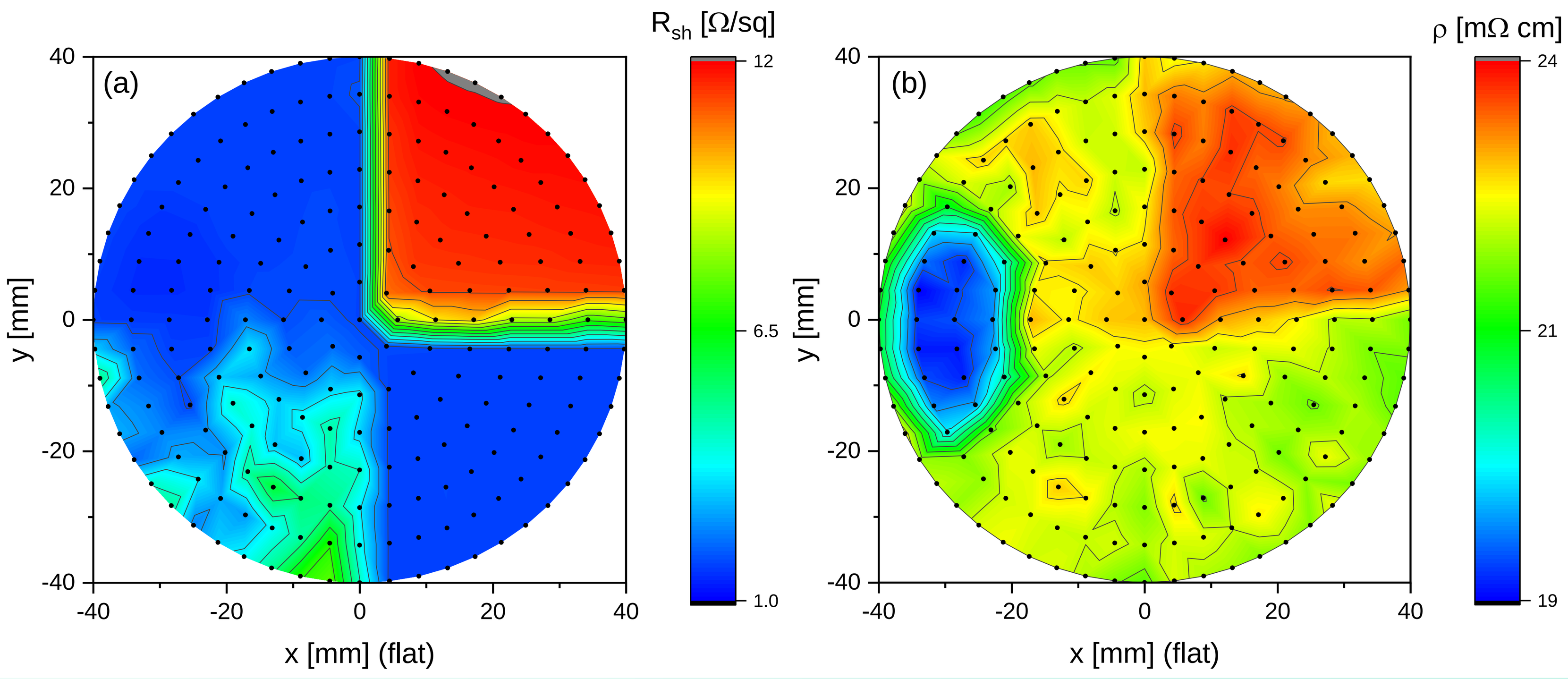
→ Positive effect of post-implant laser anneal to forward voltage of studied JBS diodes

## Discussion

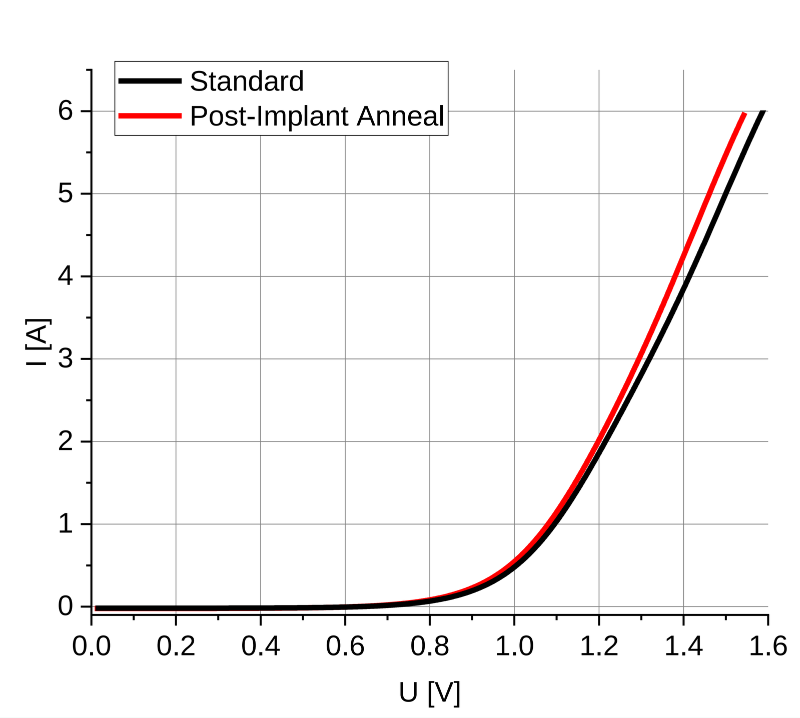
Possible explanations

- Activation of implanted dopants and recovering of lattice by laser annealing leading to a high doping near surface [2]
- Formation of carbon layer by evaporation of silicon in the top layer of silicon carbide by laser annealing [3]
- Melt-mediated phase transformation leading to 3C-SiC caused by melting and reconstructing during laser annealing [3]

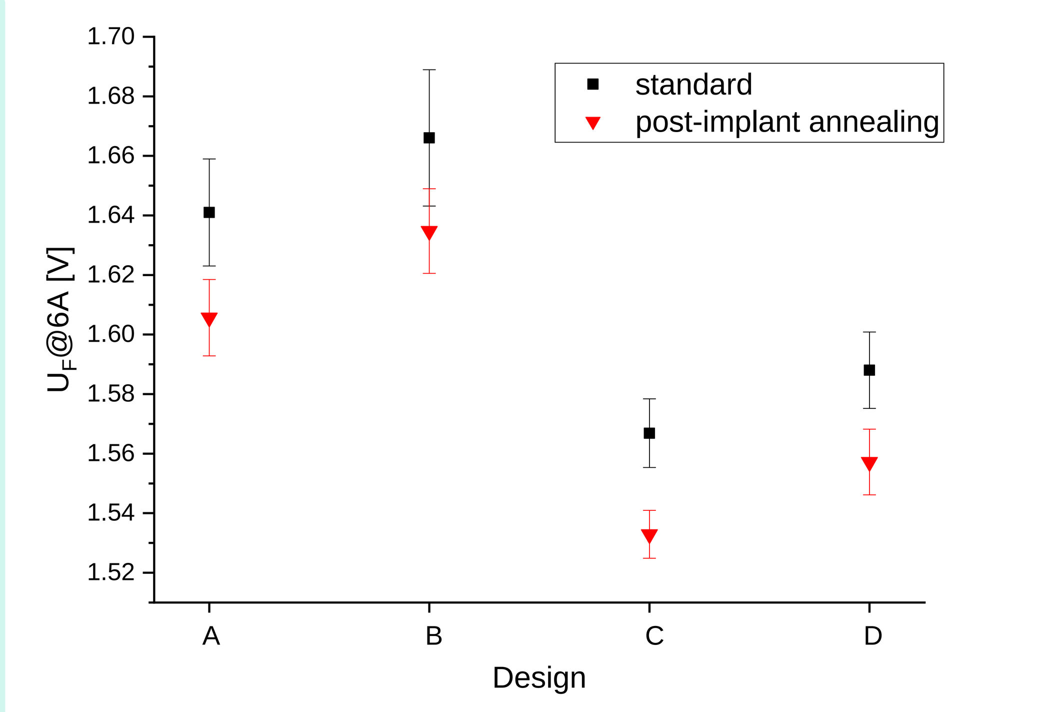
(a) Sheet resistance measurement after post-implant annealing and NiAl 2.6% sputtering and (b) specific resistance after ohmic contact formation annealing




(c) Comparison of representative forward characteristics of standard and post-implant annealed JBS diodes




(d) Forward voltages at 6 A of standard and post-implant annealed JBS diodes with different designs




## Summary

- Investigation of pulsed-laser-based tempering of backside N-implanted 4H-SiC
- Voltage drop of 40 mV at 6 A for post-implant laser annealed JBS diodes compared to standard independent of p⁺ stripe design
- Further work necessary like TEM analysis or SIMS measurements

## References


- [1] T. Kimoto, "Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications", IEEE Press, Wiley, Singapore (2014)
- [2] C. Boutopoulos, "Laser annealing of Al implanted silicon carbide: Structural and optical characterization". Applied Surface Science 253, Athens (2007)
- [3] I. Choi, "Laser-induced phase separation of silicon carbide", Nature communications, Daejeon (2016)


Fraunhofer IISB

Forschungsfabrik Mikroelektronik Deutschland

Bundesministerium für Bildung und Forschung

LEB