Trench Gate Integration into Planar Technology for Reduced On-resistance in LDMOS Devices

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1. Objectives

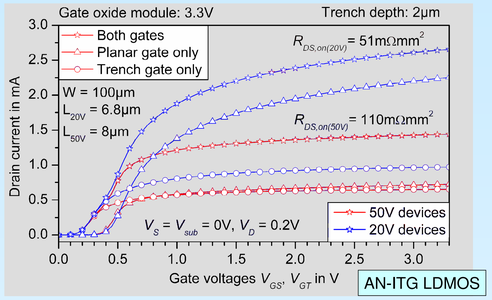
- **Feasibility investigation on the incorporation of trench gate topology into LDMOS devices for reduced $R_{DS,on}$**
  - 50V and 20V fully-isolated LDMOS devices
  - Different gate oxide modules for maximum gate voltages of 3.3V, 5V and 20V, respectively
- **Development of integration concept with limited number of additional process steps**
- **Compatibility of trench gate integration without changes to the given process flow and well implants**

2. Motivation

- **Current density is limited by resistance of the drift region at the surface (under planar gate/field plate)**
- **Further improvement of state-of-the-art LDMOS devices for smart-power applications is difficult to achieve**
  - Sophisticated RESURF design required to ensure adequate performance; re-design is time-consuming
  - Novel concepts must not deteriorate performance of other device types (e.g. logic, memory)
    - Process flow cannot easily be changed
  - ➔ Recent high-current trench gate LDMOS designs cannot be used in foundry processes
    - Well implants (dose, energy, sequence) must remain unchanged (proper RESURF design)
- **Existing, self-isolating LDMOS devices offer a deep n-well which may be usable for current conduction**
- ➔ Combine planar LDMOS technology and trench gate technology suitable for integration in smart-power ICs

4. Simulation Results

- **Transfer characteristics**



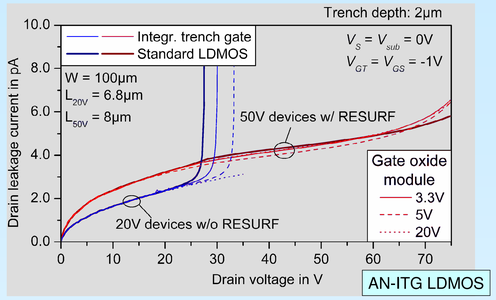
- Surface and trench gates can be independently controlled
- Significantly reduced $R_{DS,on}$ due to trench gate integration

- **Summary of $R_{DS,on}$ reduction for 20V and 50V LDMOS devices**

	Gate oxide module		
	3.3V	**5V**	**20V**
20V Devices			
Standard LDMOS (L = 6.8µm)	62	63	58
ITG-LDMOS (L = 8.3µm)	64 (+3%)	66 (+5%)	59 (+2%)
AN ITG-LDMOS (L = 6.8µm)	51 (-21%)	53 (-16%)	48 (-17%)
50V Devices			
Standard LDMOS (L = 8.0µm)	217	209	145
ITG-LDMOS (L = 9.5µm)	153 (-29%)	151 (-28%)	117 (-18%)
AN ITG-LDMOS (L = 8.0µm)	110 (-49%)	110 (-47%)	94 (-36%)
Absolute $R_{DS,on}$ values are in mΩ•mm²			

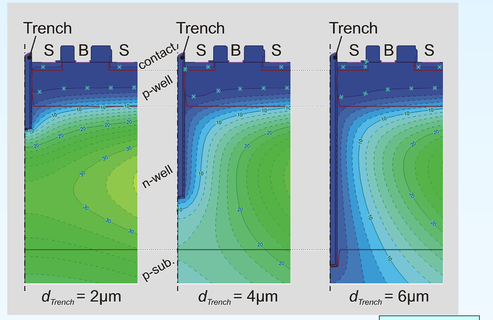
- Benefit of trench gate integration diminishes for thicker gate oxides
  - Trench drift resistance dominates for high gate voltages

- **Blocking characteristics**



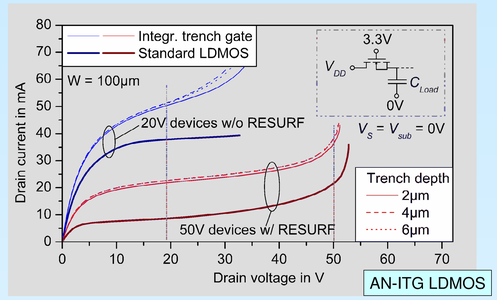
- Increase in drain leakage current not visible below 25V and 70V for the 20V and 50V LDMOS devices, respectively
  - ➔ Existing design of wells (RESURF) is suitable for trench gate integration

- **Electrostatic potential near trench region for 50V device with 20V gate oxide**



- Impact of vertical field plate is clearly visible with increasing trench depth

- **Output characteristics (Kirk-effect limitations)**



- Integrated trench gate LDMOS exhibits acceptable immunity to Kirk effect
- Higher device currents in ITG LDMOS result in lower breakdown voltage
  - Trench drift region (n-well) has not been optimized for current conduction

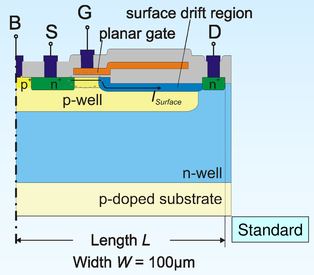
- **Summary of maximum drain voltages for 20V and 50V LDMOS devices**

	Gate oxide module		
	3.3V	**5V**	**20V**
20V Devices			
Standard LDMOS	24.9V	32.2V	27.4V
ITG-LDMOS	28.1V	> 35V	34.9V
AN ITG-LDMOS	29.5V	> 35V	34.0V
50V Devices			
Standard LDMOS	53.2V	53.2V	52.8V
ITG-LDMOS	50.8V	52.3V	50.8V
AN ITG-LDMOS	50.7V	52.8V	50.8V

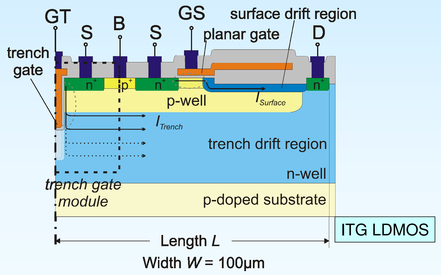
- 20V devices (w/o RESURF): Vertical field plate increases breakdown voltage
- 50V devices (w/ RESURF): Higher drain currents reduce breakdown voltage

3. Integration concept

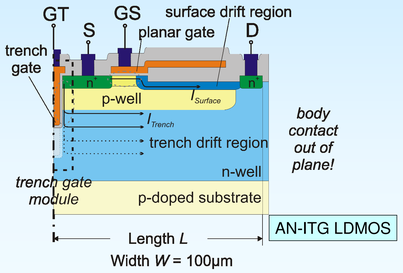
- **Standard LDMOS device (schematic)**
  - Concept currently in production



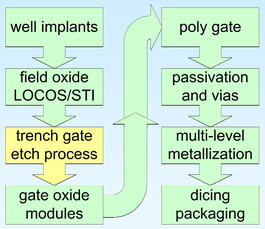
- **Integrated Trench-Gate (ITG) LDMOS device**
  - Trench gate module is integrated into source → device area increases



- **"Area-Neutral" Integrated Trench-Gate (AN-ITG) LDMOS device**
  - Trench gate module replaces body contact → identical device area, but body-switching restricted



- **Extended process flow**



- **Trench gate integration requires added RIE etch module (but no changes to flow)**

5. Conclusions

- **Integration of trench gate technology into an existing LDMOS layout is feasible**
  - Significant reduction of $R_{DS,on}$ is achievable
  - Blocking behavior is not deteriorated
  - Immunity to Kirk effect is satisfactory
  - ITG LDMOS devices can be fabricated without changes to process flow or to well implants (RESURF design)
  - Existing LDMOS devices remain operational → extended library
- **Verification of simulation results by demonstrator fabrication is currently underway**
- **Further optimization of integration scheme is under investigation**