BEYOND SIC POWER DEVICES AND TECHNOLOGY –
NOVEL HIGH TEMPERATURE SIC CMOS 1 MICRON TECHNOLOGY

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Content

- Motivation
  - Latest Power Electronics Development
  - Exploiting benefits of SiC technology beyond Discrete Power Devices
- SiC CMOS technology: Circuits for Harsh Environments
  - PMOS device technology and performance
  - SPICE Modelling and design kits
- SiC CMOS circuits
  - Sensing and signal conditioning at high temperature
  - Lateral Power Devices and Process Modelling
  - Integrated SiC Gate Drivers for next-generation Power Electronics
- Conclusion and Outlook: SiC Quantum Electronics beyond 4mK operation

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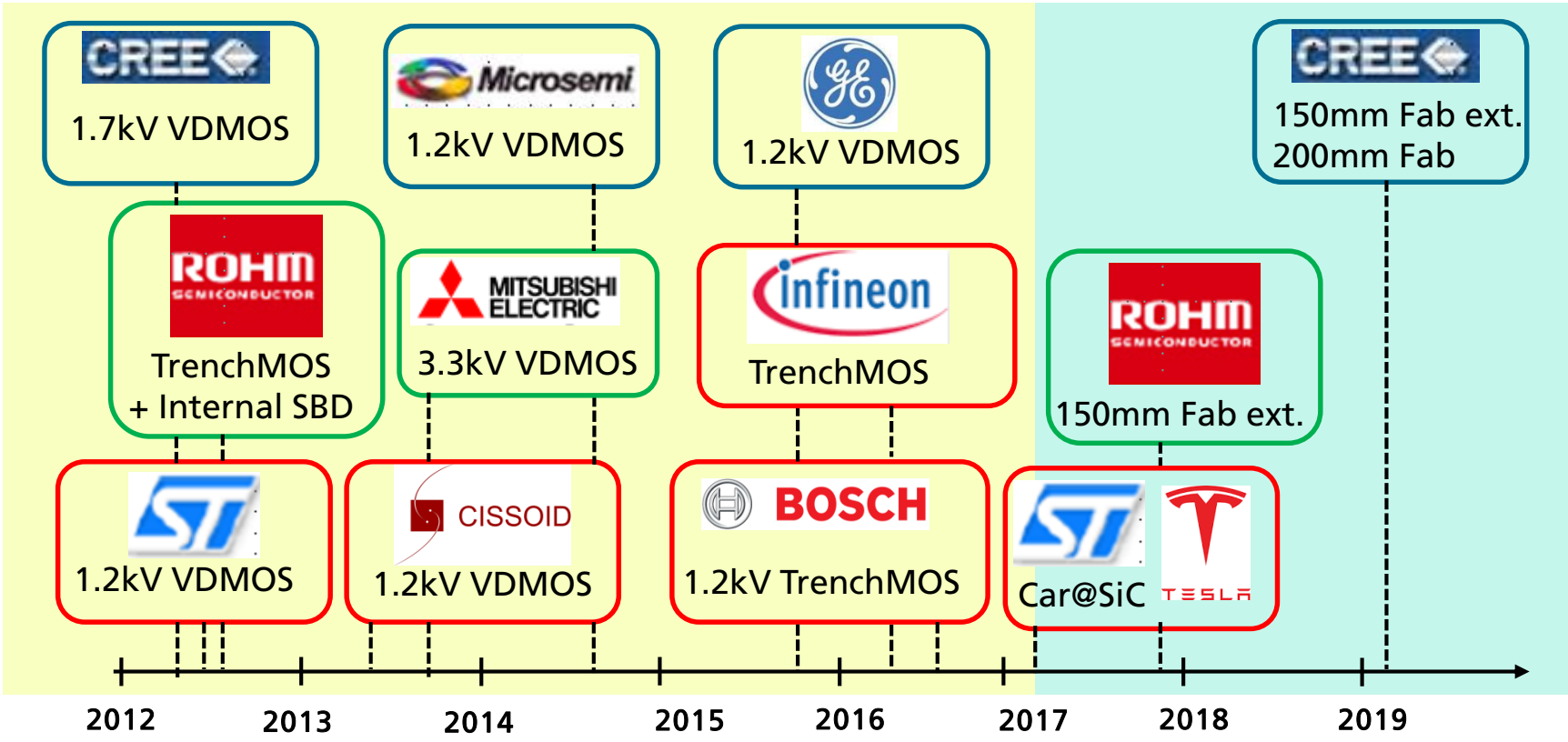
Volume fabrication of 1.2kV/1.7kV MOSFETs

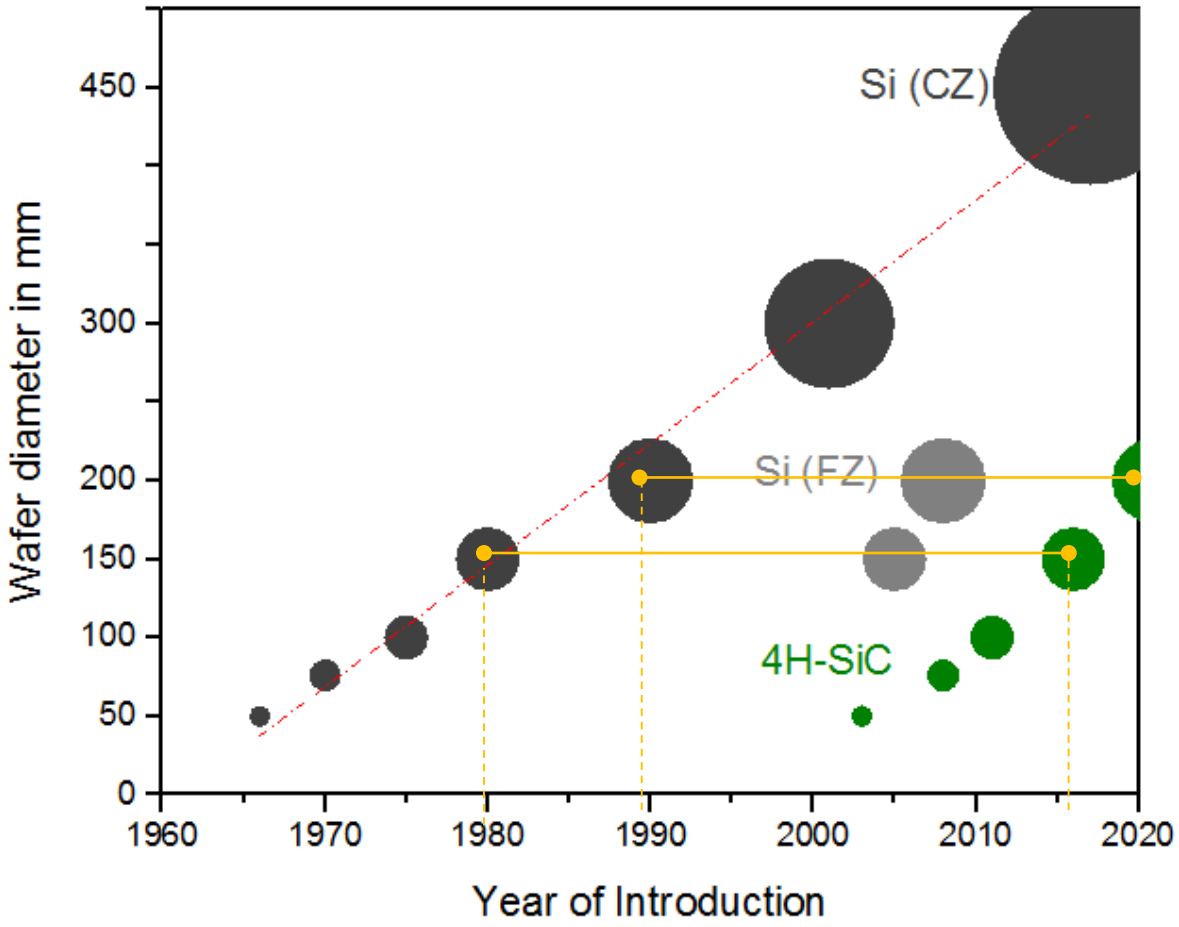
- Recent SiC MOSFET device activities/innovations



→ Transition from R&D to **ramp-up** around the globe
New SiC technologies beyond Power MOSFETs await!

Exploiting benefits of SiC Power Device technology

- Comparison to silicon technology



Significant effort to increase SiC wafer diameter

4H-SiC technology:

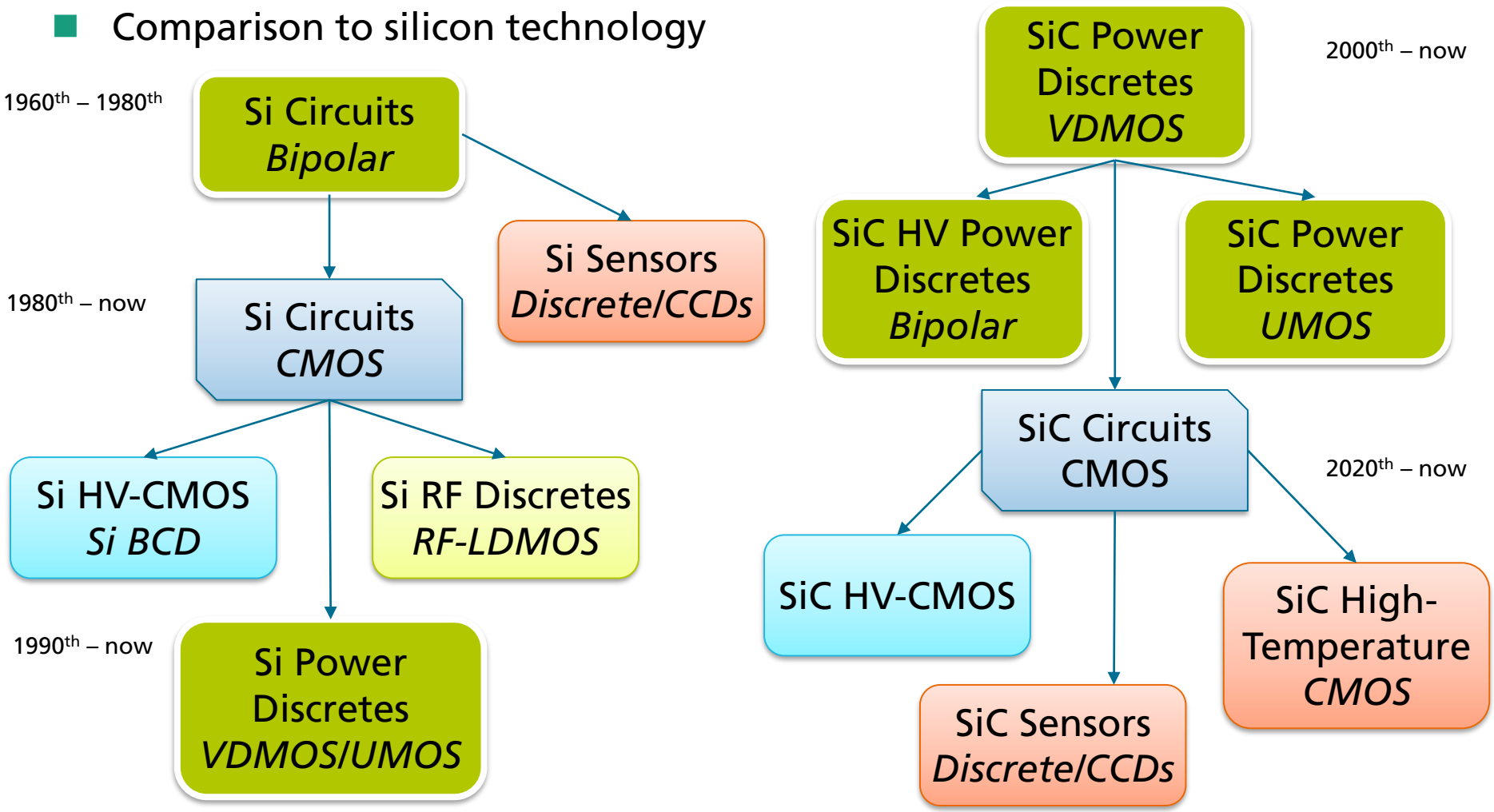
150mm: 1980th silicon era

200mm: 1990th silicon era

Silicon concepts in SiC: Shorter developments

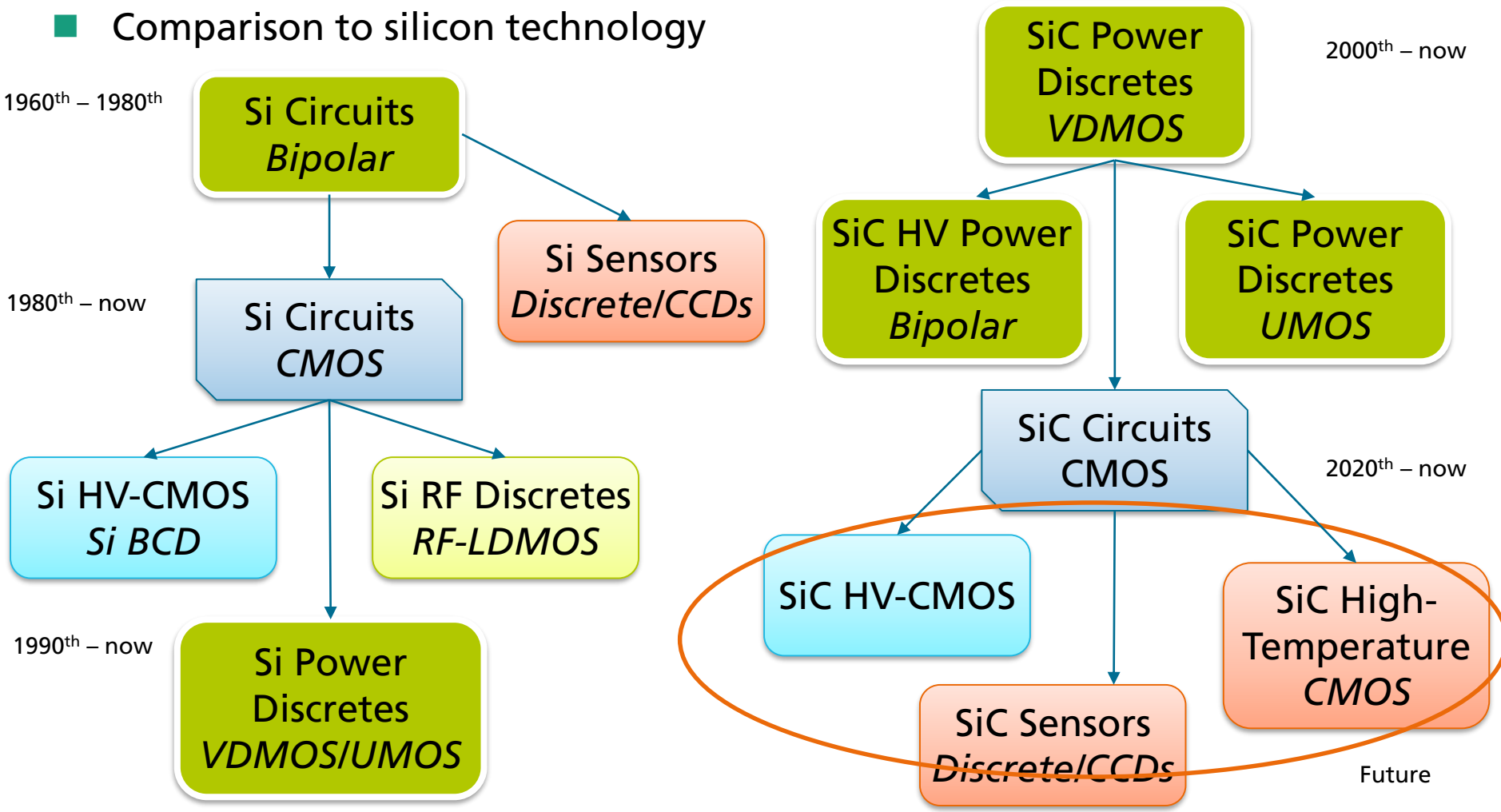
Exploiting benefits of SiC Power Device technology

- Comparison to silicon technology



Exploiting benefits of SiC Power Device technology

- Comparison to silicon technology



SiC CMOS: High temperature beyond Silicon

- Wide application range

- Bulky
- Expensive

- Unreliable
- Inaccurate

- Unreliable
- Inefficient

Energy Industries	Geothermal	Oil & Gas Exploration	Industrial Gas Turbines	Aircraft Engines	Automotive Engines
Required Sensing Temperatures	 375°C	 275°C	 600°C	 600°C	 300°C
Desired Sensing Measurands	• Pressure • Temperature • H_2S • Strain	• Pressure • Temperature • Hydrocarbon • Strain	• Pressure • Temperature • Flame speed • Acceleration	• Pressure • Temperature • Flame speed • Acceleration	• Pressure • Temperature • Flame speed • O_2

Harsh Environment Sensor Cluster, University of California, San Diego

Power Electronics

Integrated Gatedriver:

- Current
- Temperature

- High switching frequencies
- Reliabilty

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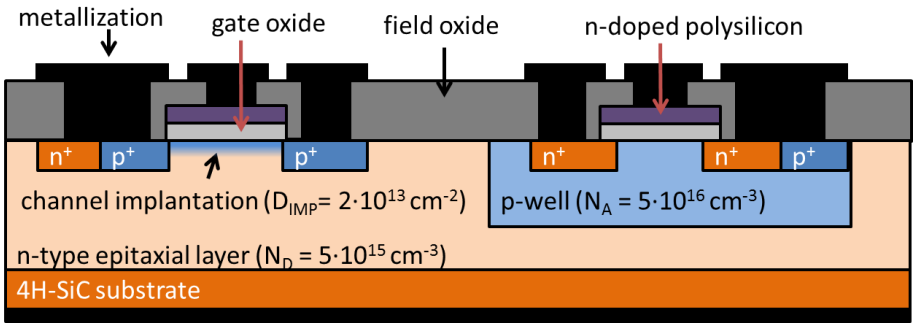
High temperature electronics beyond Silicon

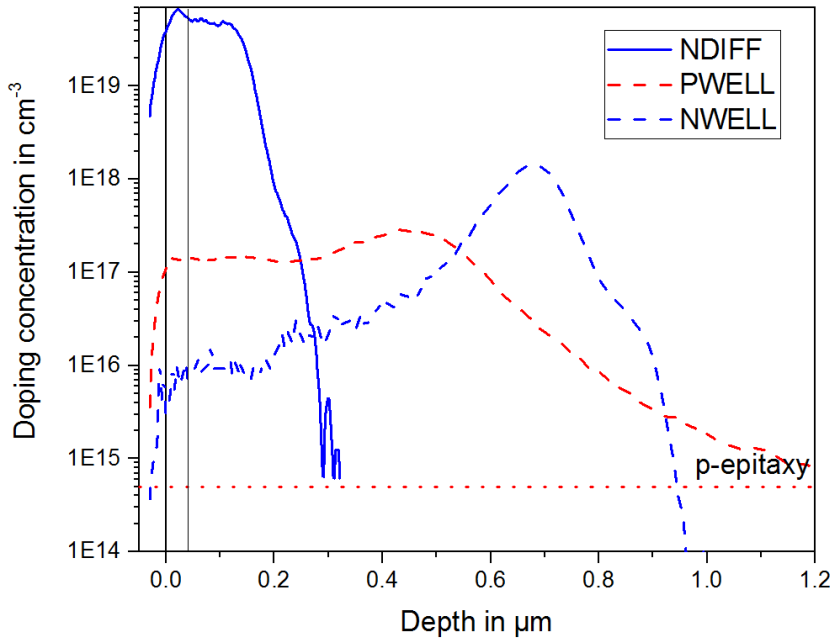
- SiC MOS devices can be operated beyond 300°C
  - Addition of PMOS transistors beyond power electronics
    - Enables well-known silicon topologies: CMOS circuits

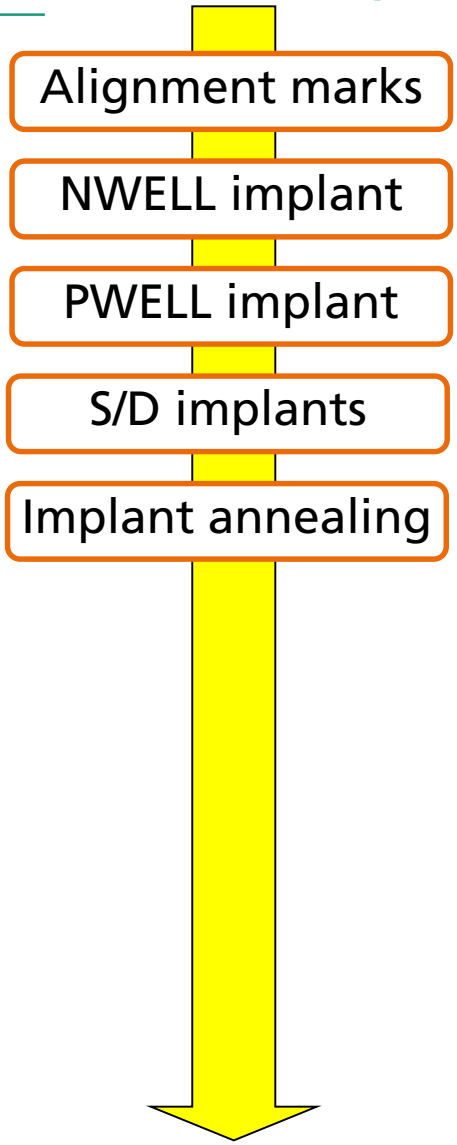


  - High temperature circuits using “SiC power technology”
    - High temperature sensing
    - Signal amplification and conditioning
  - Challenges: Optimization of pMOS transistors, high-temperature stability, MPW design capability (Fab-less + Foundry concepts)

Triple-well SiC CMOS 1P1M high-temperature technology

- Process modules
  - Triple well SiC CMOS with 2 implantations!
    - Retrograde doping profiles possible
      - NMOS+PMOS transistors high-side capable

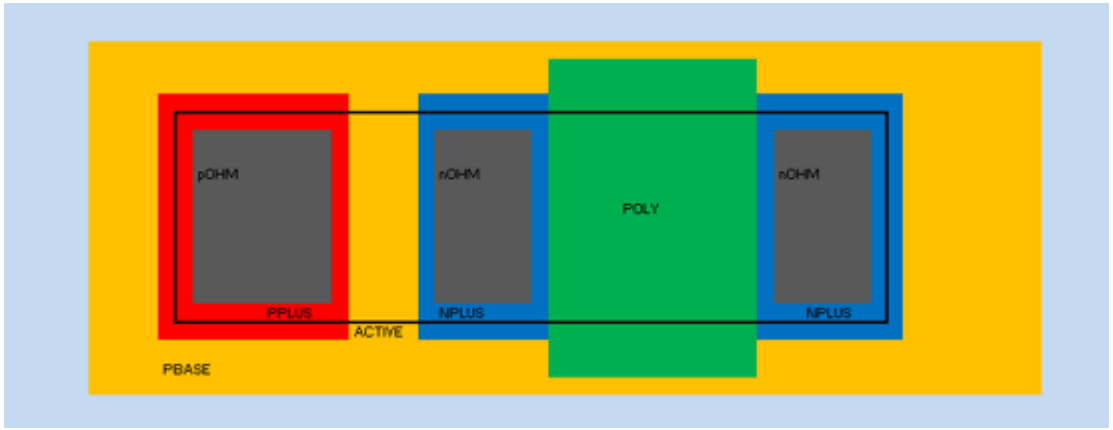


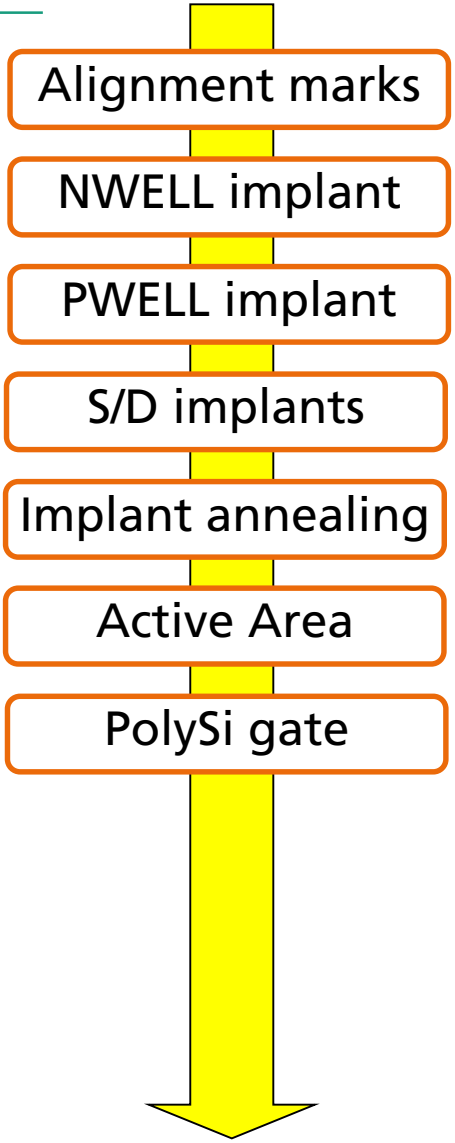


Triple-well SiC CMOS 1P1M high-temperature technology

- Process modules
  - Self-aligned gate module cannot be implemented (SiC requires implant anneal before oxide!)
    - Active area for gate width control possible
    - Additional gate area overlap has to be included

      → Increased gate-source/gate-drain capacitance

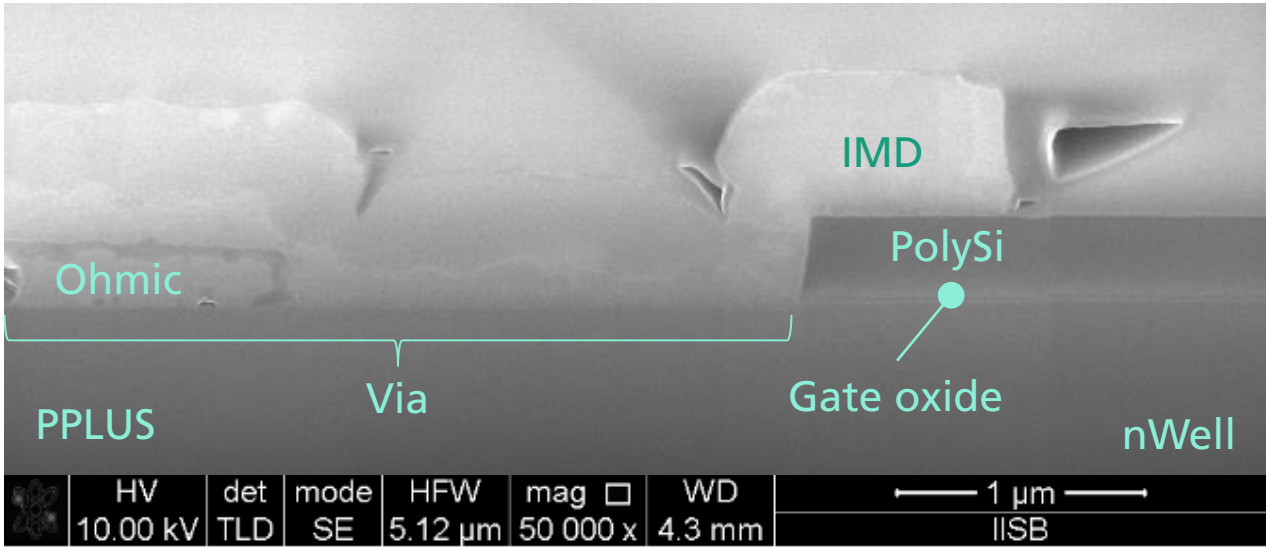


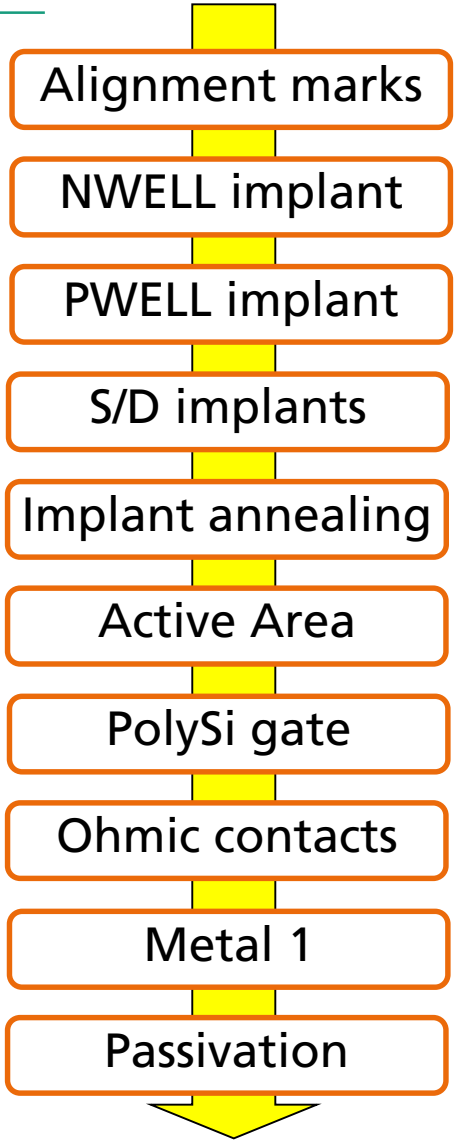


Triple-well SiC CMOS 1P1M high-temperature technology

- Process modules
  - Pt-based metallization stack
    - Ohmic contact is sensitive to degradation
    - Passivation using SiN or a-SiC:H

FIB/SEM image of 20/6µm SiC PMOS transistor after Ohmic contacts



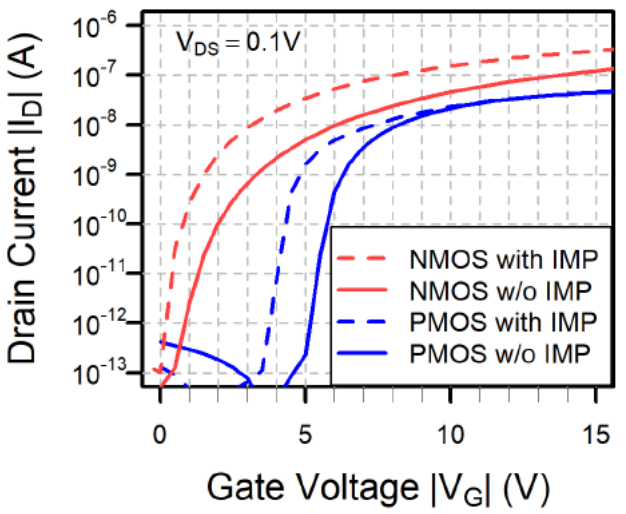


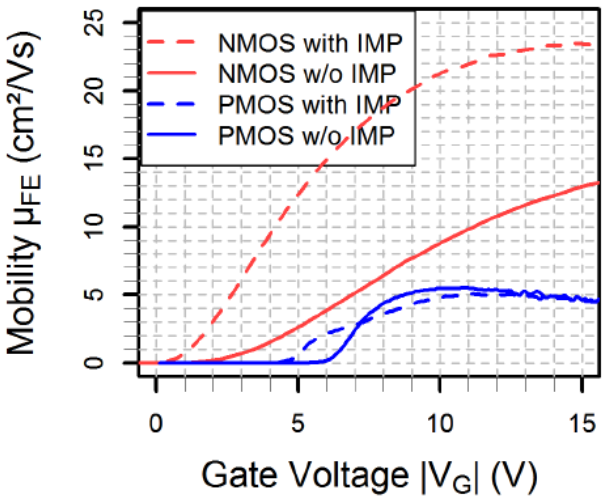
High temperature electronics beyond Silicon

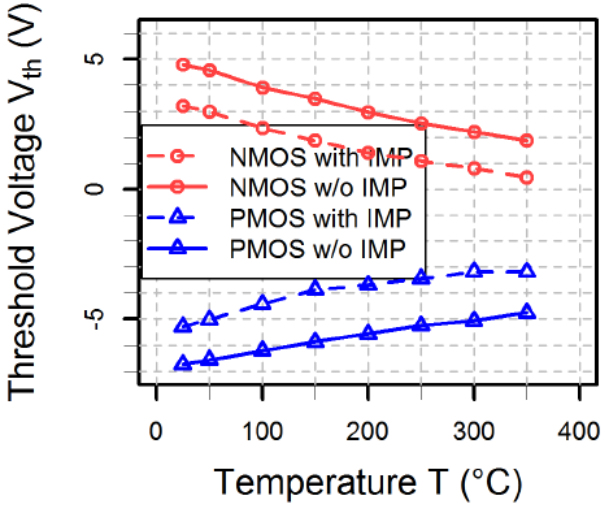
- "Triple-well" SiC CMOS 1P1M technology beyond 300°C
  - NMOS and PMOS transistors fabricated by ion implantation (w/ channel)
  - Polygate process, 1Pt metal
  - Ohmic contact formation using NiAl and RTP
    - NMOS V_{Th}: 1.5V – PMOS V_{Th}: -6.0V, contact resistance

→ There is still room for improvement!

*Albrecht et al., Mat. Sci. Forum **1004** (2020) 1123–1128*

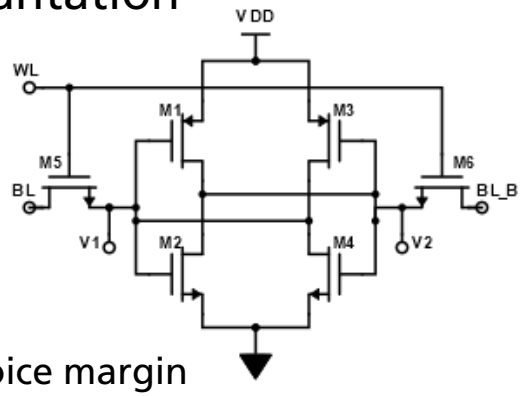




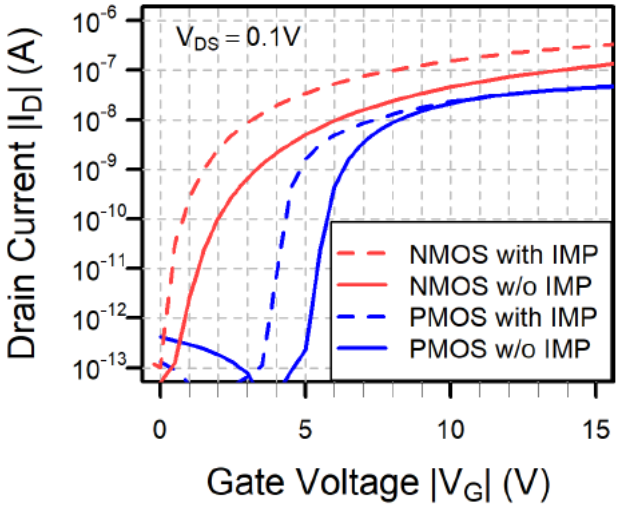


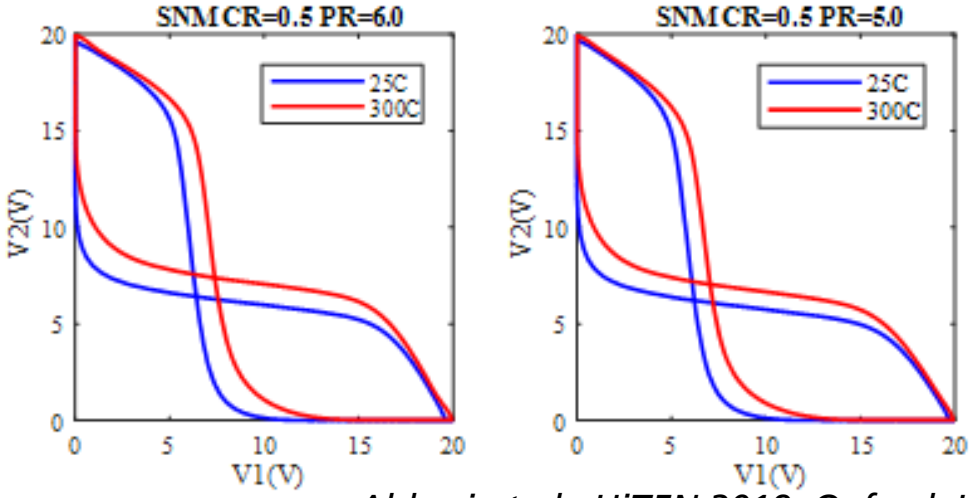
High temperature electronics beyond Silicon

- "Triple-well" SiC CMOS 1P1M technology beyond 300°C
  - NMOS and PMOS transistors fabricated by ion implantation
  - Polygate process, 1Pt metal
  - Logic circuit example (base functionality)
    - High temperature SRAM capability with low leakage current demonstrated



SNR: Static noice margin

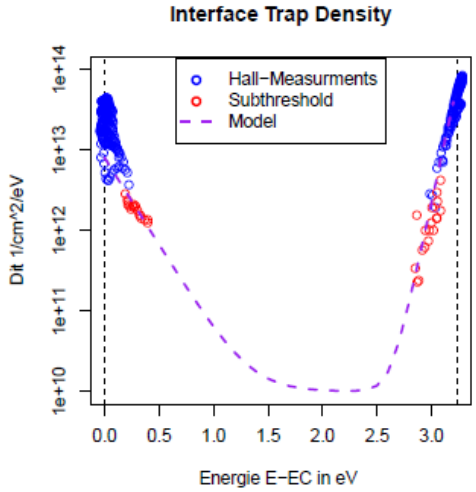


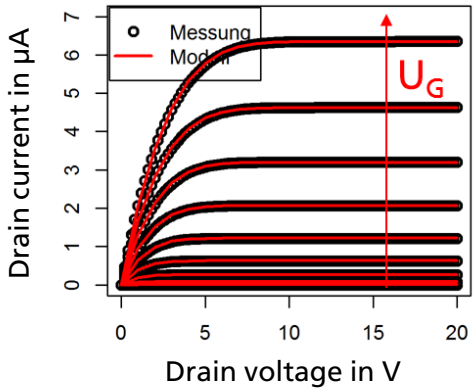


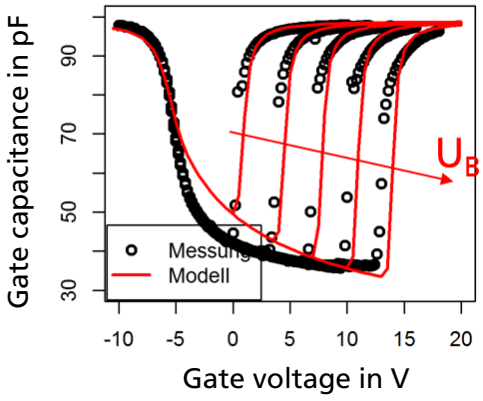
Abbasi et al., HiTEN 2019, Oxford, UK

Modelling of SiC CMOS technology

- Physical SPICE modelling for fast CMOS technology prototyping
  - Characterization of primitive devices (not IVs)
  - Extraction of physical and geometrical parameters
    - E.g. Interface state density, channel length
  - Modelling of device performance and comparison
  - SPICE Optimization:
    Fast BSIM model based on physical models



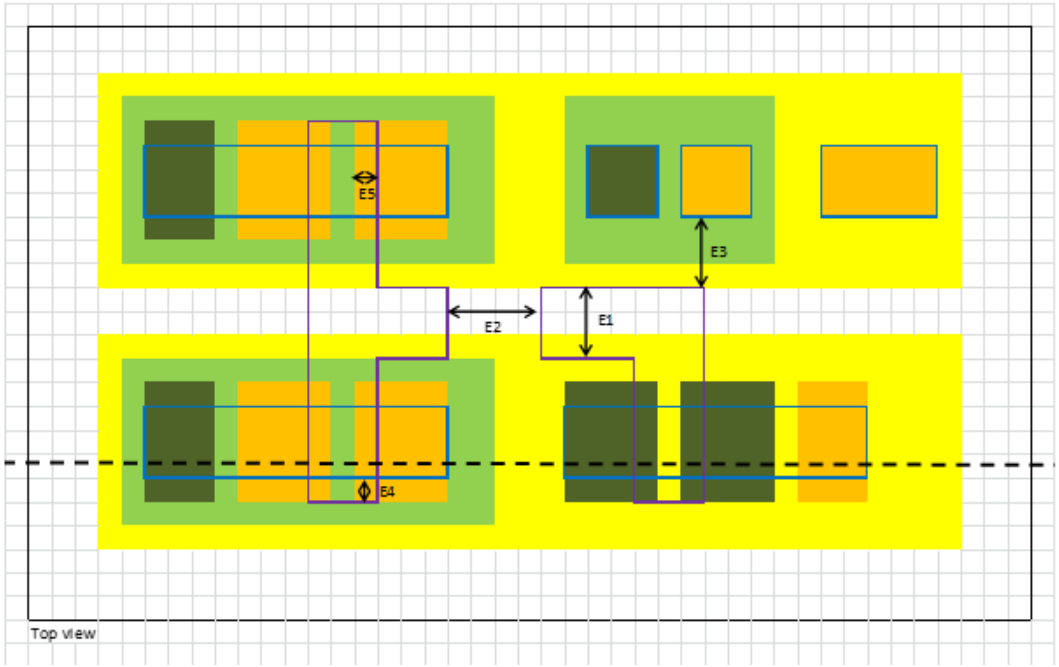




Unpublished work

Process development kit and multi project wafer runs

- PDK: Combination of process technology, device performance and circuit evaluation
  - Physical SPICE modelling for fast CMOS technology prototyping
  - Design rule check (DRC), e.g. Poly gate layer



Poly1

- **E1 Minimum size 3 µm**
- **E2 Minimum spacing 3 µm**
- **E3 Spacing to Active 2 µm**
- **E4 Gate Extension 2 µm**
- **E5 Poly over p+/n+: 1µm**

  - Incorporated into Layout software

Process development kit and multi project wafer runs

- PDK: Combination of process technology, device performance and circuit evaluation
  - Physical SPICE modelling for fast CMOS technology prototyping ✓
  - Design rule check (DRC) ✓
  - Layout versus schematics (LVS) and Electric rule check (ERC) ✓
  - Circuit examples / Design library for proven design
    - Design IP

- Prerequisite for MPW (multi-project wafer) services
  - Combination of different circuit designs ✓
  - Leveraging R&D cost across several partners ✓
  - Continuous technology improvement using dedicated process wafers ✓
    - Process IP

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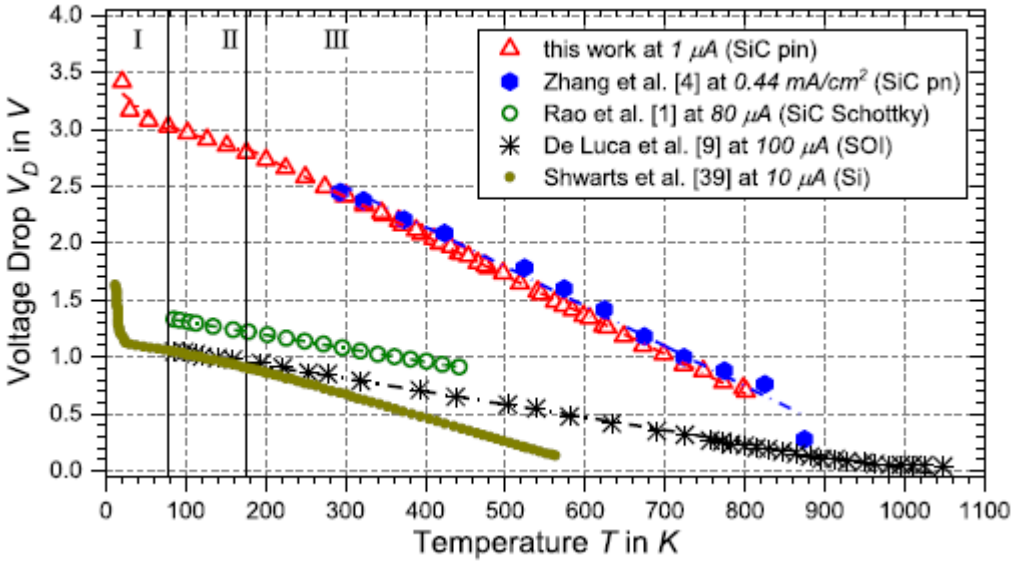
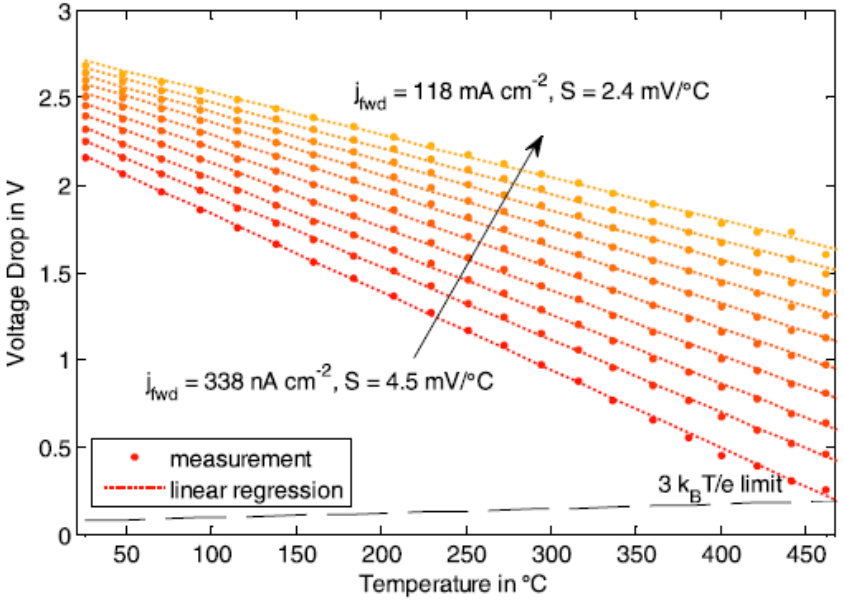
High temperature electronics beyond Silicon

- Accurate temperature sensing beyond 300°C (and down to 80K)
  - Capability demonstrated using stand-alone pin-structures
  - Wide temperature range with excellent linearity
  - Sensitivity up to 4.5 mV/K





*C. Matthus et al., IEEE Sensors J. **19** (2019) 2871-2878*

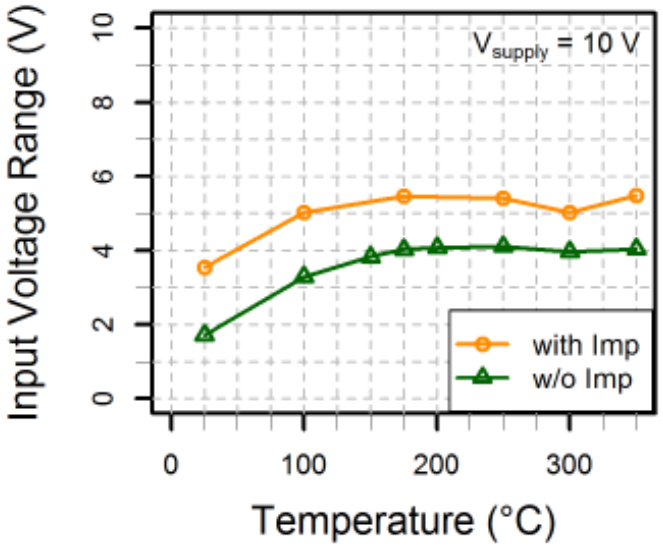
C. Matthus et al., IEEE Trans. Electron Dev. 64 (2017) 3399-4404

Fraunhofer IISB

High temperature electronics beyond Silicon

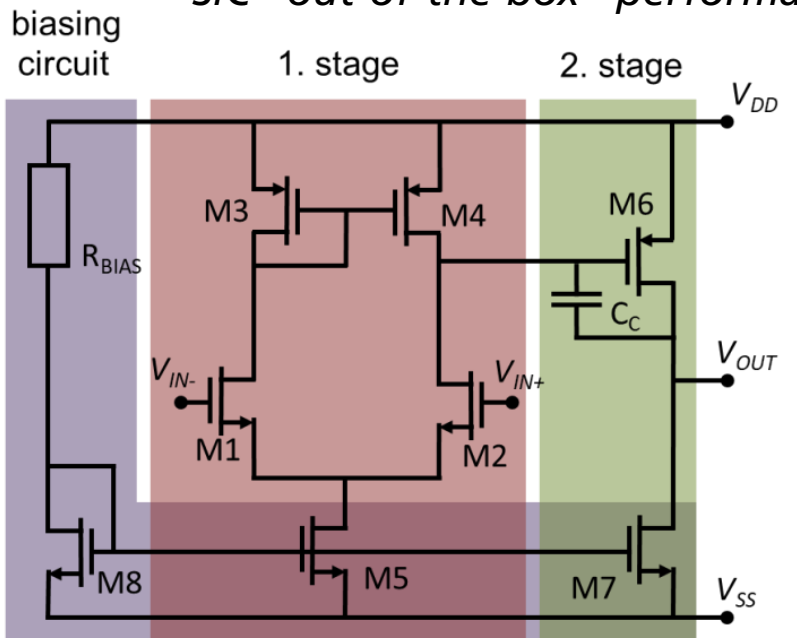
- Example: SiC High-temperature operational amplifier
  - Challenge: Evaluating low current/voltages
  - Signal conditioning at elevated temperatures
    - 20V, 10V, 5V variants

transistor	type	W/L in µm/µm
M1, M2	n	40/6
M3, M4	p	200/6
M5, M7, M8	n	225/6
M6	p	400/6



*Albrecht et al., Mat. Sci. Forum **1004** (2020) 1123–1128*

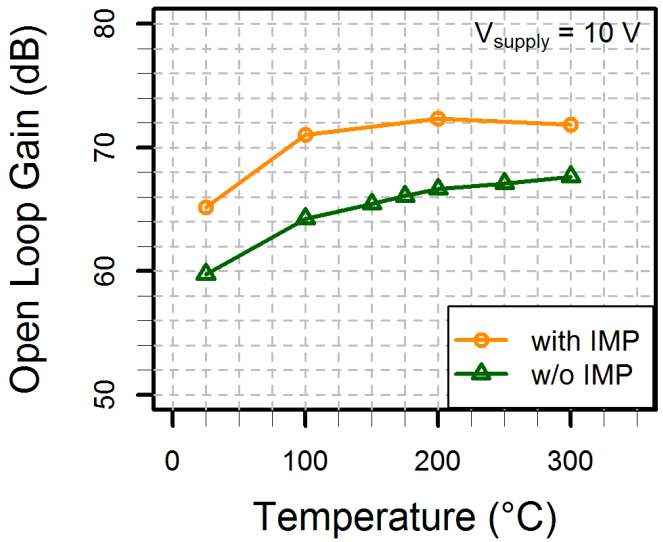
SiC "out-of-the-box" performance



Fraunhofer IISB

High temperature electronics beyond Silicon

- Example: SiC High-temperature operational amplifier
  - Signal conditioning at elevated temperatures
    - 20V, 10V, 5V variants
    - Sensor reading: Improved SNR by pre-amplification at high-temperature



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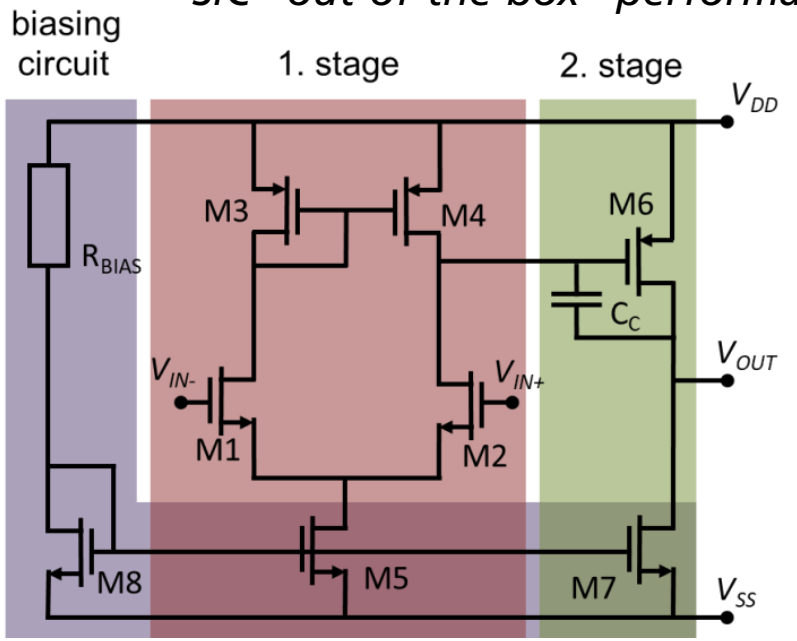
SiC "out-of-the-box" performance

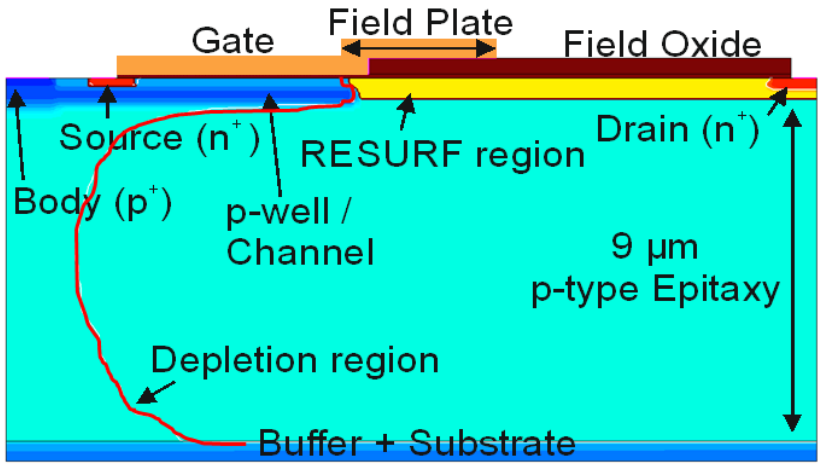


Fraunhofer IISB

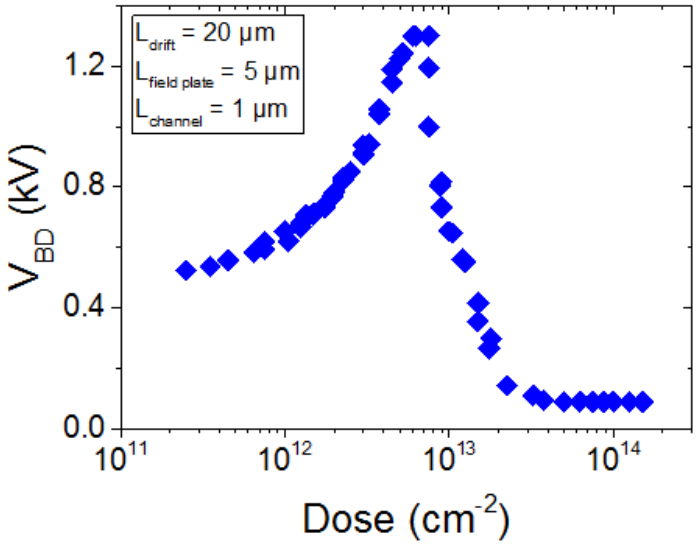
High voltage integrated circuits beyond Silicon

- Combination of CMOS and power device technology: Smart Power ICs
  - RESURF LDMOS: Another concept inspired from silicon technology

Weisse et al., ECSCRM 2018



Scheme of a lateral RESURF n-LDMOS transistor.

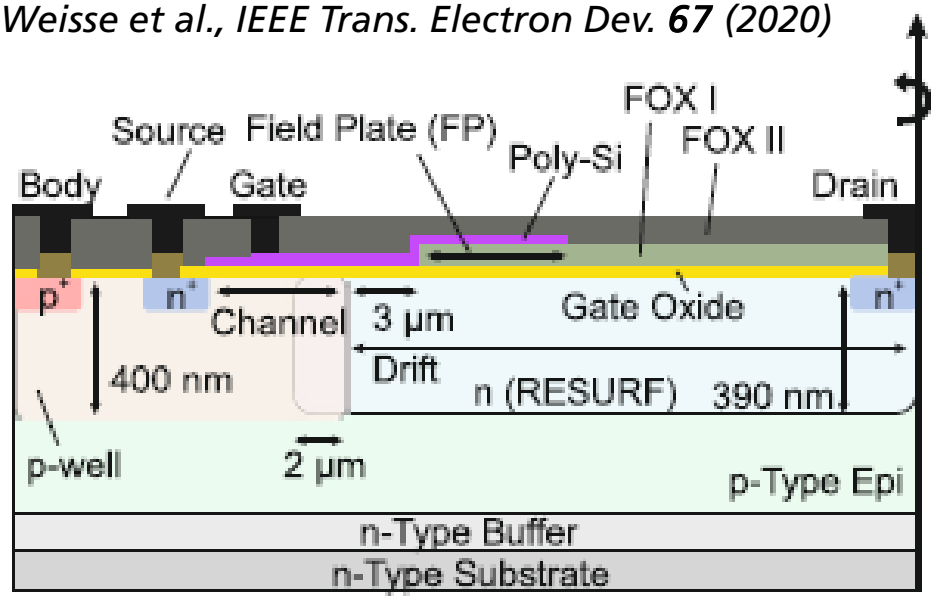


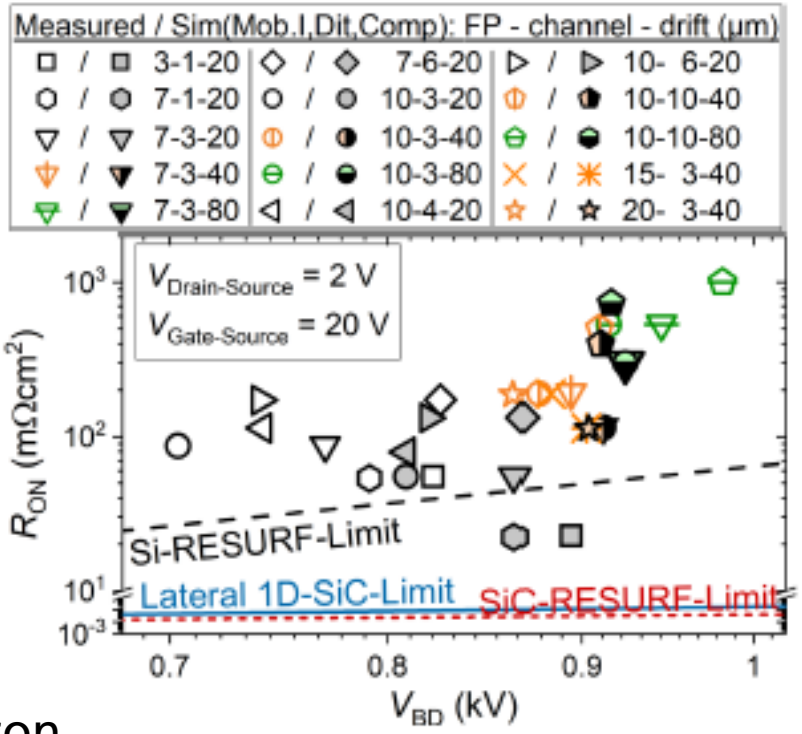
  - Achieved by N-impl. RESURF region, Optimal RESURF-dose: $6*10^{12}cm^{-2}$
    - Integration in 5/10V SiC CMOS process
    - R_{on} = 17mΩcm² @ 1.3kV

High voltage integrated circuits beyond Silicon

- Combination of CMOS and power device technology: Smart Power ICs
  - RESURF LDMOS: Another concept inspired from silicon technology

Weisse et al., IEEE Trans. Electron Dev. ***67*** *(2020)*





  - 1200V SiC LDMOS can outperform silicon

High voltage integrated circuits beyond Silicon

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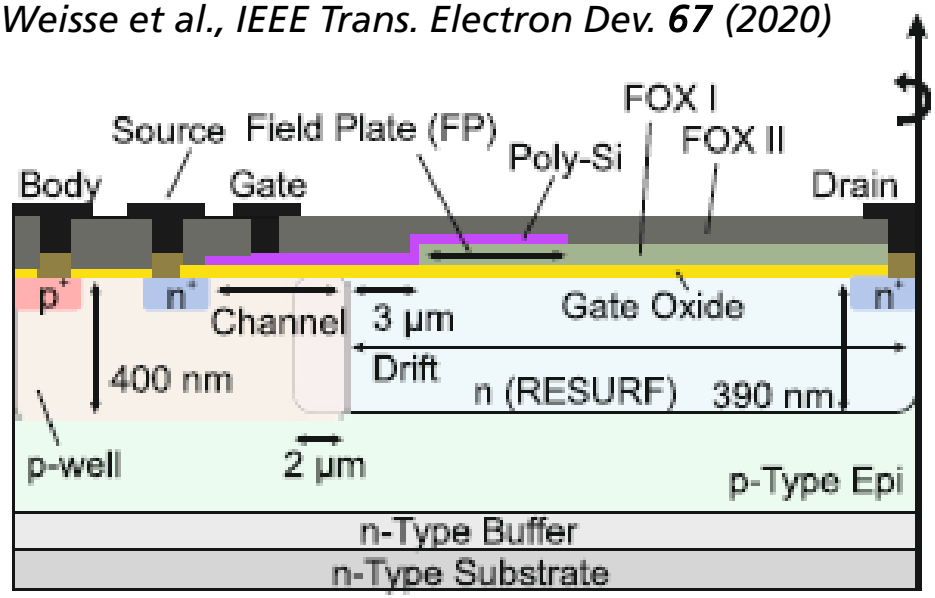
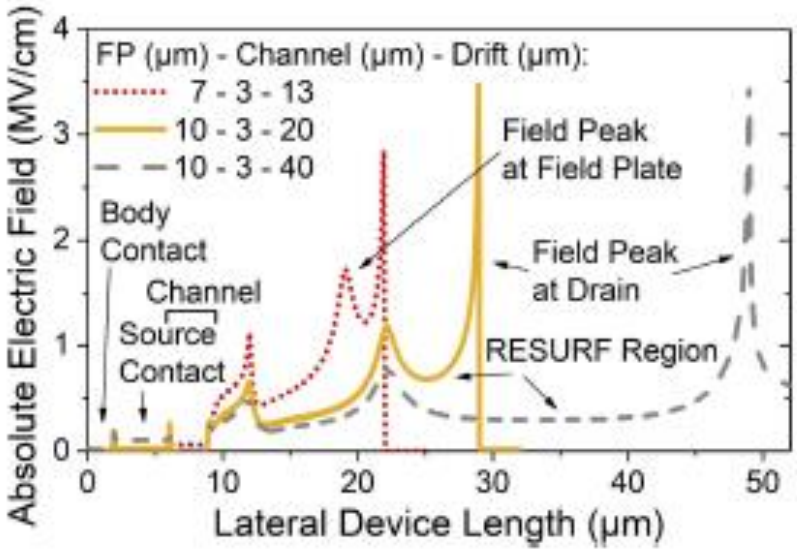


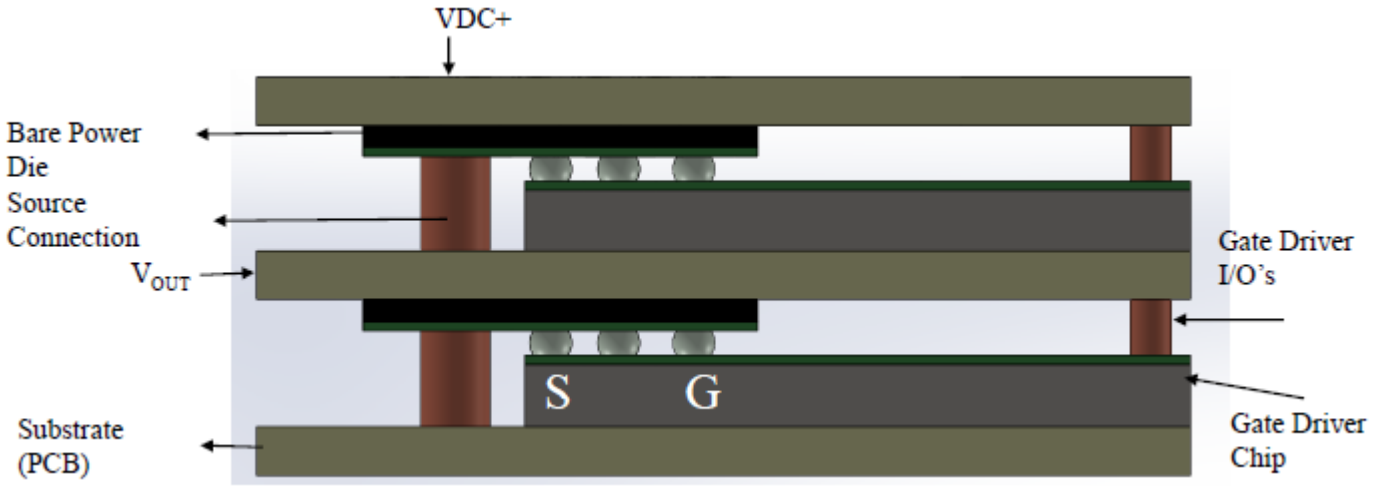


  - 1200V SiC LDMOS can outperform silicon

    → Charge balance is required (Al compensation and field spike)!

Integrated SiC Gate Drivers for Power Electronics

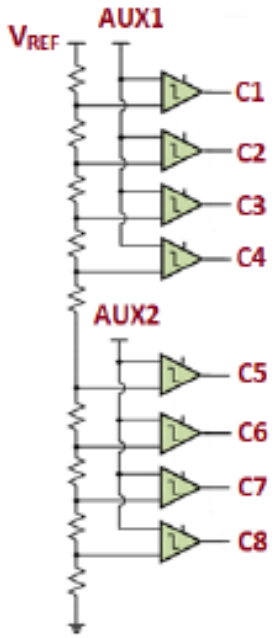
- Next-generation SiC Power Modules require low-inductive packaging
  - Implementation of gate driver into the module, e.g. Flip-chip assembly
    - Integration concept

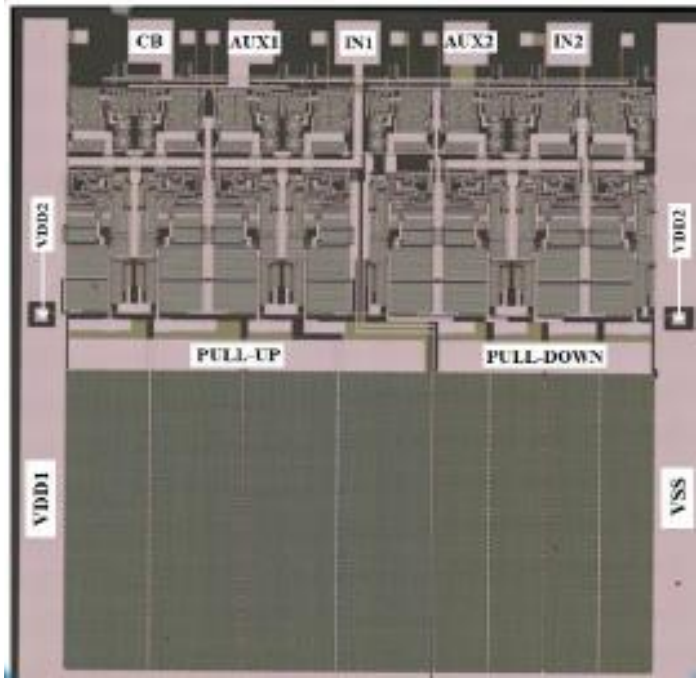


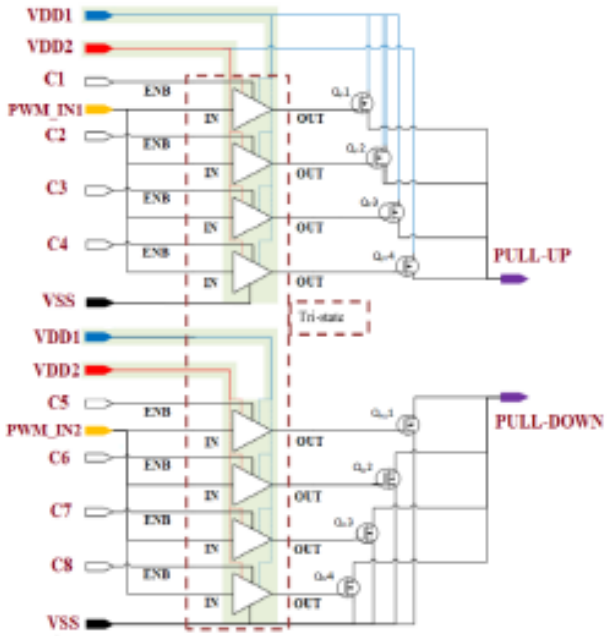
Abbasi et al., iMAPS 2020

Integrated SiC Gate Drivers for Power Electronics

- Next-generation SiC Power Modules require low-inductive packaging
  - Implementation of gate driver into the module, e.g. Flip-chip assembly
    - Circuit components and fabricated die



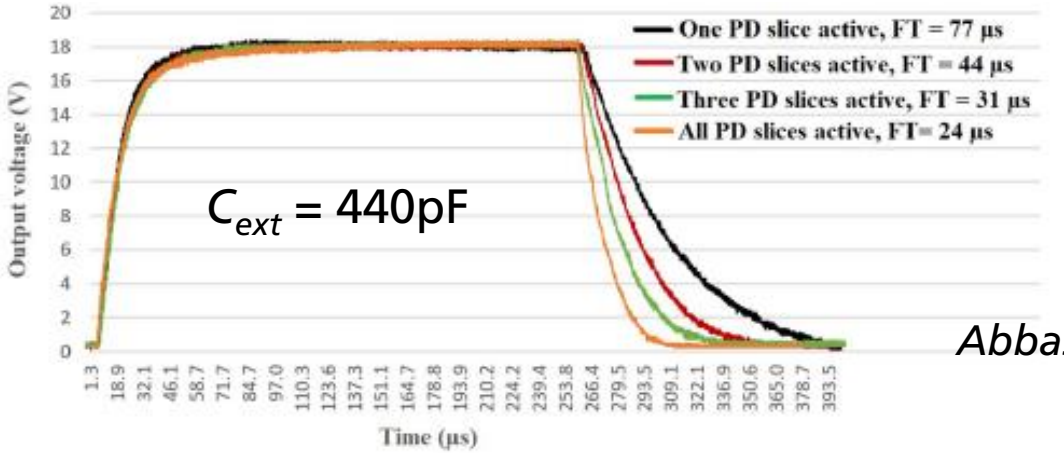




Abbasi et al., iMAPS 2020

Integrated SiC Gate Drivers for Power Electronics

- Next-generation SiC Power Modules require low-inductive packaging
  - Implementation of gate driver into the module, e.g. Flip-chip assembly
  - Gate driver performance and test results



Abbasi et al., iMAPS 2020

Parameters	Measured Results (25°C)	Measured Results (200°C)	Simulated Results (300°C)	Measured Results (300°C)
Peak Drive Current	2.26 A (sink) 1.04 A (source)	*3.52 A (sink) *1.34 A (source)	4.52 A (sink) 1.79 A (source)	*3.96 A (sink) *1.43 A (source)
Output Voltage Swing	0.35V – 18.92V	0.31V – 18.91V	0V – 18.98V	0.45V – 18.92V
Propagation Delays	895 ns (Falling)	472 ns (Falling)	191 ns (Falling)	412 ns (Falling)
	972 ns (Rising)	497 ns (Rising)	271 ns (Rising)	451 ns (Rising)
Rise and Fall Times	485 ns (Falling)	294 ns (Falling)	21 ns (Falling)	234 ns (Falling)
	876 ns (Rising)	678 ns (Rising)	103 ns (Rising)	595 ns (Rising)

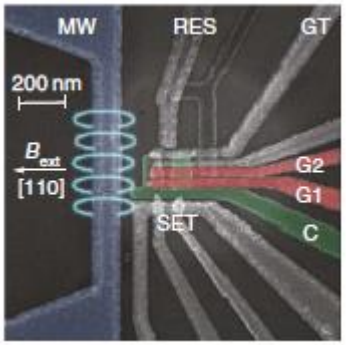
Content

- Motivation
  - Latest Power Electronics Development
  - Exploiting benefits of SiC technology beyond Discrete Power Devices
- SiC CMOS technology: Circuits for Harsh Environments
  - PMOS device technology and performance
  - SPICE Modelling and design kits
- SiC CMOS circuits
  - Sensing and signal conditioning at high temperature
  - Lateral Power Devices and Process Modelling
  - Integrated SiC Gate Drivers for next-generation Power Electronics
- Conclusion and Outlook: SiC Quantum Electronics beyond 4mK operation

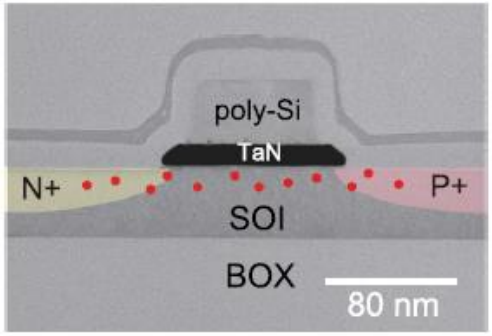
Outlook: Room-temperature quantum operation

- SiC Quantum Electronics beyond cryogenic operation
  - Silicon qbits demonstrated up to 1.1K *(C.H. Yang et al., Nature 2020)*
  - Metal-oxide-silicon dots

    Henson et al., Nature Nanotechnology 15, (2020) 13–17



    - Coupling of electron spins with 29Si spins and transfer of electrons to neighboring dots
    - Cryogenic temperatures, typ. < 4K
  - Tunneling field effect transistors
    - Stronger confinement due to spin-blockade eff offering electron confinement up to 0.3eV
    - Cryogenic temperature, 5–10K demonstrated



Ono et al., Scientific Reports volume 9 (2019) #469

Outlook: Room-temperature quantum operation

- SiC Quantum Electronics beyond cryogenic operation
  - Silicon qbits demonstrated up to 1.1K *(C.H. Yang et al., Nature 2020)*
  - SiC color centers can be stable at room temperature
    - Reduced cooling effort
    - Suitable for mass products
    - Technology platform available

→ A new application for SiC?

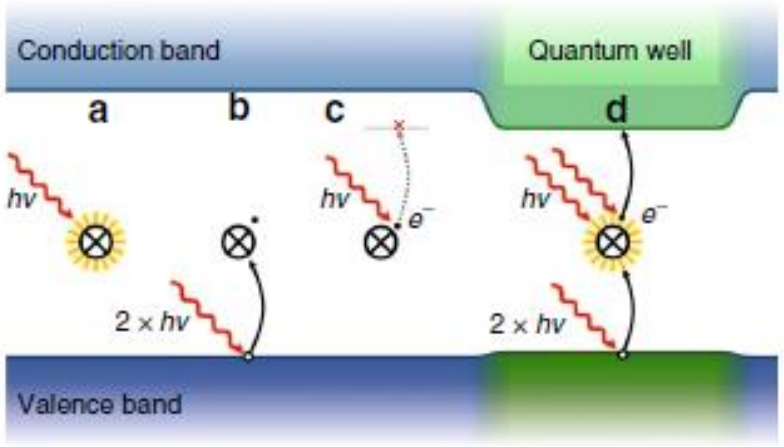
	Si	GaAs	diamond	6H/4H-SiC	3C-SiC
Index	3.5	3.4	2.4	2.6	2.6
Band gap [eV]	1.12	1.42	5.5	3.05/3.23	2.36
Quantum emitter	-	Quantum dots	Color centers	Color centers	Color centers
Room T emission	-	No	Yes	Yes	Yes
Wafer-scale substrates	Yes	Yes	No	Yes	Yes
Sacrificial layer	SOI	AlGaAs	-	-	Si

Table 1 – Properties of substrates commonly used in photonics.

Radulaski, Vučković, Stanford Univ. 2020

Outlook: Room-temperature quantum operation

- SiC Quantum Electronics
  - Divacancies (PL1–PL4 IDed, PL5–PL8?)
- Silicon vacancy in SiC
  - Frank-type stacking fault + PL5–PL8



Ivady et al., Nature Communications 10 (2019) # 5607

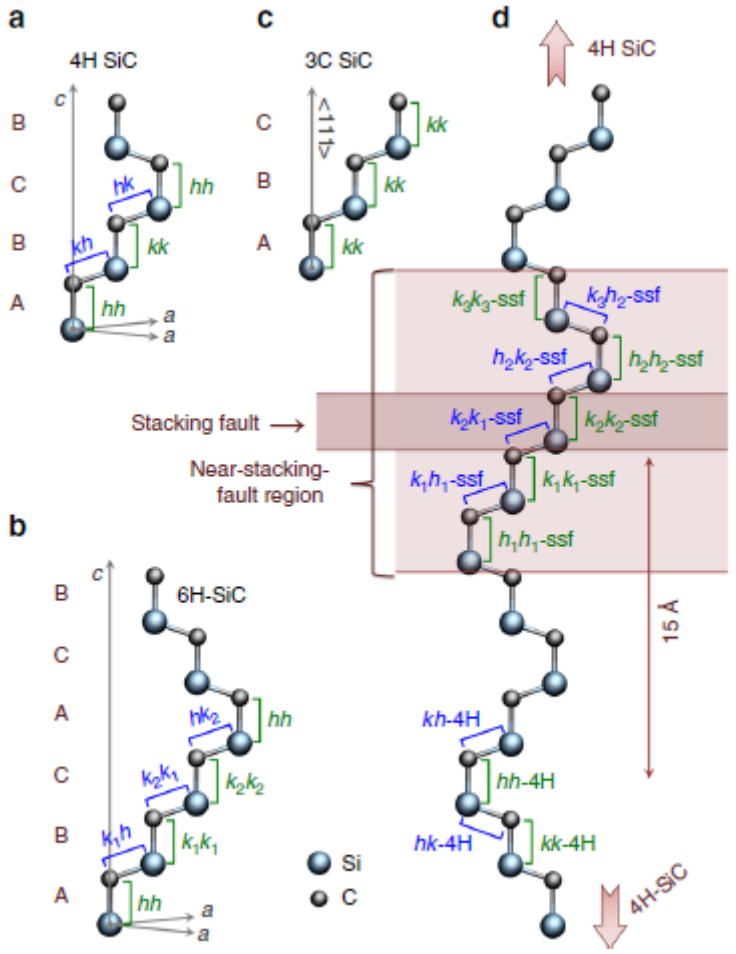
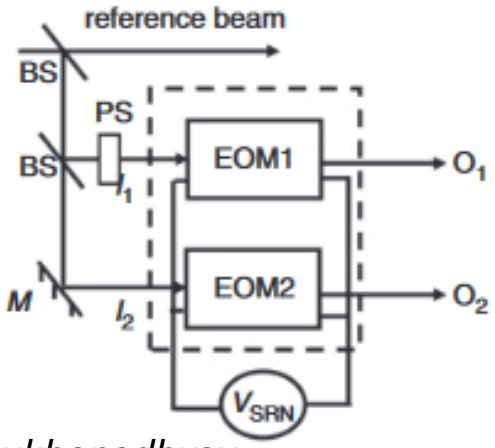


Fig. 2 Common SiC polytypes and structure of a stacking fault in 4H-SiC.

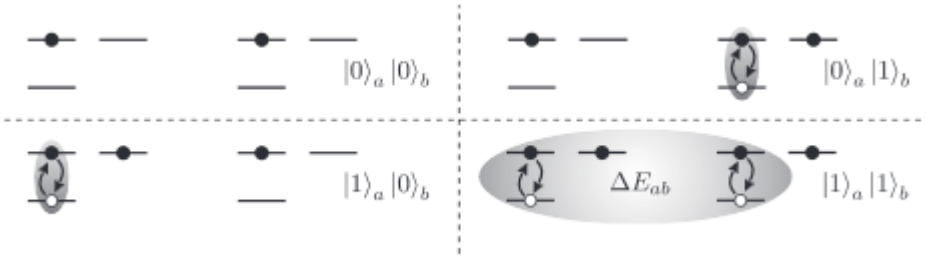
Outlook: Room-temperature quantum operation

- Silicon carbide quantum gates
  - Logic building blocks for quantum electronics, e.g.
    - $\sqrt{NOT}$ (SRN) ⇔ Superposition
      (Reversible, pure-optical quantum gate)
    - $\sqrt{SWAP}$ ⇔ Entanglement
    - Pauli-X gate / Pauli-Y gate
    - Pauli-Z-gate ⇔ Phase shift gate

      → Optical interference



Dey and Mukhopadhyay, Electronic Letters 53 (2017) 1375–1377



- Combination with ordinary logic circuits
  - 4H SiC Quantum CMOS technology?

    → Quantum Conversion (QADCs) circuits for interfacing

Pazy et al., Europhys. Lett. 62 (2003) 175-181

Conclusion

- Conclusion
  - SiC process technology enables CMOS circuits
    - Harsh environment applications (Room temperature can be harsh!)
    - New possibilities in power electronics
    - Technology development has just started
    - PDKs ensures MPW capability and accessibility
  - SiC CMOS technology enabling quantum electronic applications?
    - Templates for Quantum Dots
    - Logic gates and quantum computing
  - Matching application pull and technology push beyond Si CMOS → Innovation

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And…

Thank you for

Your attention!