Effect of Bulk Potential Engineering on the Transport Properties of SiC MOSFETs: Characterization and Interpretation

V. Uhnevionak,[1,5,a*] A. Burenkov,[1,5] C. Strenger,[1,5] G. Ortiz,[3,5] V. Mortet,[4,5]
E. Bedel-Pereira,[3,5] F. Cristiano,[3,5] A. J. Bauer,[1,5] P. Pichler[1,2,5]

[1] Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany

[2] Chair of Electron Devices, Cauerstrasse 6, 91058 Erlangen, Germany

[3] CNRS-LAAS, 7 avenue du colonel Roche, 31400 Toulouse, France

[4]Institute of Physics, Academy of Sciences of the Czech Republic, v.v.i, Prague 8, Czech Republic

[5]The Wide Bandgap Semiconductor Alliance (WISEA)

[a]viktoryia.uhnevionak@iisb.fraunhofer.de

Keywords: 4H-SiC MOSFETs, interface traps, bulk traps, depth dependence.

Abstract. The effect of bulk potential engineering on the transport properties in the channel of SiC MOSFETs has been studied. For this purpose, n-channel SiC MOSFETs have been manufactured with different background doping concentrations and characterized electrically at room temperature by current-voltage as well as by Hall-effect measurements. To interpret the measurements performed, numerical simulations have been carried out using Sentaurus Device of Synopsys. The main finding of the simulation analysis is that the change in the depth of the band-bending has to be considered to explain the doping dependence of SiC MOSFET characteristics.

Introduction

Because of its unique physical and electronic properties, silicon carbide has become a promising material for the development of field-effect transistors for high-power electronics. However, due to the low drain current and mobility in the channel, the commercial use of SiC-based MOSFETs is still limited. Their low performance is mainly explained by the high density of charged traps at the SiO_2/SiC interface which results in strong Coulomb scattering. To increase the channel mobility, the impact of Coulomb scattering at the charged interface traps has to be reduced. Currently, the main strategy for a reduction of the aforementioned scattering mechanism is based on methodologies for the passivation of the interface traps. However, it is important to note that the intensity of Coulomb scattering doesn't depend on the amount of traps by itself but on the amount of traps which are occupied and charged. The lower the amount of the charged interface traps, the lower the intensity of Coulomb scattering and the higher the channel mobility. In addition to the passivation methodologies, the amount of charged interface traps which affect the performance of MOSFETs can be controlled by changing the background doping concentration N_A. A change in the background doping concentration corresponds to a change in the bulk potential ϕ_B. By changing the bulk potential and, as a consequence, the band-bending required to invert the MOSFET channel, the occupation of the traps located at the interface also changes. Along that line, it has been suggested that a reduction of the background doping concentration leads to a reduction of the density of charged interface traps and with them of Coulomb scattering [1, 2]. The reduced density of charged interface traps was then taken as an explanation for the mobility increase in lateral SiC MOSFETs found experimentally. However, it was found in the current work that an explanation of the increased channel mobility requires a broader view of the effects associated with a decreasing N_A.

Experiments

To study the effect of bulk potential engineering, lateral n-channel 4H-SiC MOSFETs have been fabricated on p-type 4°-off 4H-SiC (0001) Si-face substrates with aluminum concentrations N_A of

$1 \cdot 10^{15}$ cm^{-3}, $1 \cdot 10^{16}$ cm^{-3}, and $5 \cdot 10^{16}$ cm^{-3}. The channel length and width of the MOSFETs were 500 µm and 80 µm, respectively. To obtain Al concentrations of $1 \cdot 10^{16}$ cm^{-3} and $5 \cdot 10^{16}$ cm^{-3}, box-shaped, p-type wells were fabricated by multiple Al-implantations into the epitaxial layer which had a concentration of $1 \cdot 10^{15}$ cm^{-3}. The gate oxide with a thickness of 25.5 nm was grown by thermal oxidation in N_2O atmosphere at 1550 K and annealed at the same temperature in N_2 ambient. To characterize the MOSFETs electrically, current-voltage and Hall-effect measurements were performed at room temperature. The source-drain voltage V_D in the measurements was set to 0.1 V and the gate voltage was varied between 0 and 20 V. The details of the fabrication process as well as the measurement setup can be found elsewhere [3].

Results and Discussions

To interpret the doping dependence of the electrical measurements performed, a TCAD simulation analysis has been carried out with Sentaurus Device of Synopsys. Firstly, the current-voltage characteristics have been numerically simulated using the Near-Interface Trap (NIT) and mobility degradation models. A full description of them will be given in [4]. For an accurate description of the interface traps energetically located near the conduction band of SiC, their density versus trap energy was extracted from the Hall-effect measurements of the studied MOSFETs and used directly in the simulations [5]. A comparison of the simulated and measured drain currents is shown in Fig. 1. To correct the Hall-effect measurements, the Hall factor r_H as a function of doping concentration was evaluated for the electron transport in the channel of the SiC MOSFETs. The estimation of the Hall factor has been performed on the basis of the successful simulations of the current-voltage characteristics using our previously developed method [6]. The results of the calculation are shown in Fig. 2.

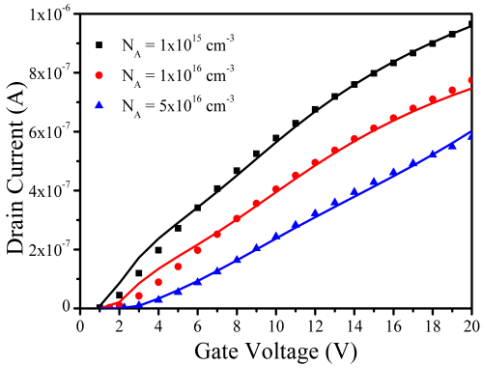

Fig. 1. Comparison of the simulated (lines) and measured (symbols) drain current.

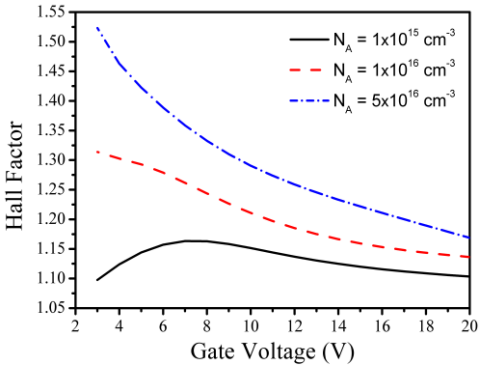

Fig. 2. Hall factor in the channel of SiC MOSFETs.

As it can be seen, the Hall factor depends not only on the gate voltage applied, as it was discussed in [6], but also on the background doping concentration of the MOSFETs. With a decrease in the doping concentration N_A, the values of the Hall factor strongly decrease which can be mainly explained by a reduction of Coulomb scattering in the channel. Taking the results in Fig. 2, the sheet carrier density n_{inv} and channel mobility μ determined from the Hall-effect measurements were corrected with the calculated r_H and compared with the simulations. The simulated n_{inv} and μ were derived from the current-voltage characteristics presented in Fig. 1. The results of the comparison are shown in Fig. 3 and Fig. 4 for the sheet carrier density and drift mobility, respectively. All the calculations in the current work have been performed in analogy to our previous one [6].

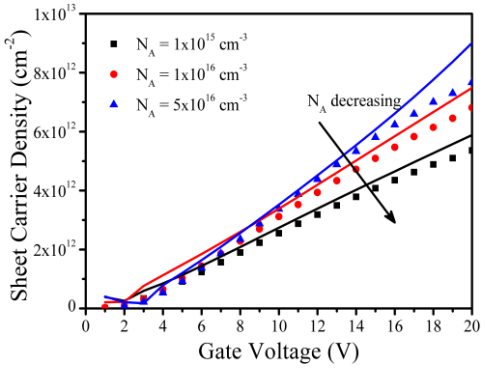

Fig. 3. Comparison of the simulated (lines) and measured (symbols) sheet carrier density.

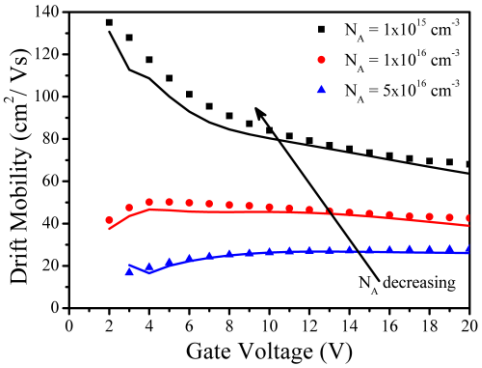

Fig. 4. Comparison of the simulated (lines) and measured (symbols) drift mobility.

A very good agreement between simulations and corrected Hall measurement has been achieved for the sheet carrier density n_{inv} as well as for the mobility μ. Analyzing the substrate doping dependence of the SiC MOSFET characteristics, it can be seen that the drain current and channel mobility, presented in Fig. 1 and Fig. 4, increase strongly with decreasing N_A while the sheet carrier density shown in Fig. 3 decreases. In MOSFETs with ideal interfaces, i.e. without interface traps, a decrease in N_A leads to an increase of n_{inv} for the same gate voltage. When there are traps, as in SiC MOSFETs, a decrease in N_A leads to a reduction of the amount of charged interface traps due to the decrease of the bulk potential. Thus, if only the impact of the charged interface traps on the transport properties in the channel of SiC MOSFETs is taken into account, n_{inv} as well as μ should increase with decreasing N_A. However, a decreasing sheet carrier density was observed for decreasing N_A values which indicates an increase in the amount of trapped electrons. Considering that the studied MOSFETs have identically fabricated gate oxides and that the implantation does not generate any additional defects which affect the MOSFET performance, as shown in [7], the higher amount of charged traps at lower N_A values is unexpected. However, this effect can be explained on the basis of a model proposed by Agarwal et al. [8]. They suggested that not only interface traps influence the performance of SiC MOSFETs but also bulk traps located in the depletion region. They further speculated that the bulk traps can be introduced during fabrication processes. Independent of their origin, the mechanisms by which they might impact on the transport properties in the channel are the same as for interface traps, namely trapping and scattering of electrons.

To understand the effect of bulk traps, the band diagrams for the MOSFETs with $N_A=5\cdot10^{16}$ cm^{-3} and $N_A=1\cdot10^{15}$ cm^{-3} have been extracted from Sentaurus Device. They are shown in Fig. 5 together with the bulk potential ϕ_B and the depletion width x_D calculated for the respective conditions.

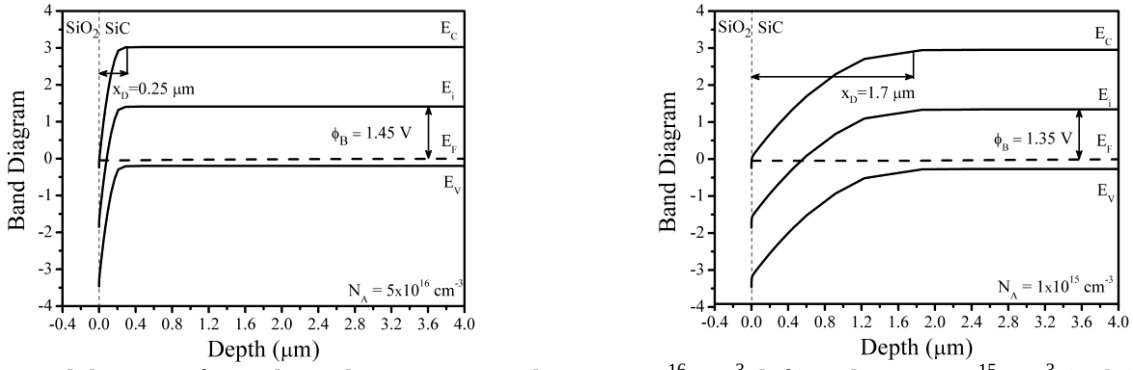

Fig. 5. Band diagrams for n-channel MOSFETs with $N_A= 5\cdot10^{16}$ cm^{-3} (left) and $N_A= 1\cdot10^{15}$ cm^{-3} (right).

Therein, ϕ_B and x_D were calculated by the formulas [9]:

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right); \qquad x_D = \sqrt{\frac{4\varepsilon_S\phi_B}{qN_A}} \tag{1}$$

where k is Boltzmann's constant, T temperature, q the elementary charge, ε_S the dielectric constant of the semiconductor and n_i the intrinsic concentration.

As it can be seen, with a decrease in N_A from $5 \cdot 10^{16}$ cm^{-3} to $1 \cdot 10^{15}$ cm^{-3}, ϕ_B decreases only from 1.45 V to 1.35 V while x_D changes strongly and shows an increase from 0.25 μm to 1.7 μm. Considering that at high doping concentrations the depletion width is small and that the inversion layer is located close to the interface, the sheet carrier density as well as the channel mobility are determined mainly by the traps located at the interface. With decreasing N_A the depletion region as well as the inversion layer become wider and more and more bulk traps will affect the electron transport in the channel of the transistor in addition to the interface traps. As a consequence, this results in the lower n_{inv} at the lower N_A, as it was concluded from the Hall-effect measurements. To explain how bulk potential engineering affects the channel mobility, several mechanisms have to be taken into consideration. First, the additional charged bulk traps at lower values of N_A will additionally contribute to Coulomb scattering of the channel electrons. However, since the density of the bulk traps is usually much smaller than the local density of the traps at the interface, Coulomb scattering at the former should be much smaller than at the latter. Second, due to the decrease of the bulk potential with decreasing N_A, the amount of the charged interface traps will decrease. Finally, since the thickness of the inversion layer increases for lower values of N_A, the depth dependence of the mobility in the transistor plays also a role. As it was shown by Potbhare [10], moving from the interface into the bulk of the SiC crystal, the charged interface traps have less and less impact on the mobility due to the quick decrease of the Coulomb potential. All these effects together explain the strong increase in μ when the background concentration is lowered. Thus, the influence of bulk potential engineering on the transport properties in the channel of SiC MOSFETs can be explained by the combination of several effects, as discussed above, which result in a lower sheet carrier density but in a much higher channel mobility and drain current at lower background doping concentrations.

Summary

TCAD simulations have been performed to understand the effect of bulk potential engineering on the transport properties in the channel of the lateral 4H-SiC MOSFETs. To interpret the Hall-effect measurements, the Hall factor was calculated as a function of the background doping concentration in the channel of the studied MOSFETs. A very good agreement between measurements and simulations was achieved. The results of the simulation analysis revealed that to explain the doping dependence of the transport properties in the channel of SiC MOSFETs bulk traps as well as the depth dependence of the mobility have to be considered in addition to interface traps.

Acknowledgment

This work has been carried out in the framework of the project MobiSiC (Mobility engineering for SiC devices) and supported within the Program Inter Carnot Fraunhofer (PICF 2010) by the BMBF (Grant 01SF0804) and the ANR, as well as by the J.E. Purkyne fellowship awarded to V. Mortet by the Academy of Sciences of the Czech Republic.

References

[1] S-H Ryu et al., Mater. Sci. Forum 615-617, 743 (2009).
[2] K. Matocha, Solid-State Electronics, 52, 1631 (2008).
[3] C. Strenger, "Herstellung und Charakterisierung von Metall-Oxid-Halbleiter-kondensatoren und Feldeffekttransistoren auf 4H-Siliciumcarbid", Ph.D. thesis, to be published.
[4] V. Uhnevionak, Ph.D. thesis to be submitted to the Technical Faculty of the University Erlangen-Nuremberg.
[5] G. Ortiz et al., "Impact of fabrication process on electrical properties and on interfacial density of states in 4H-SiC n-MOSFETs studied by Hall effect", to be published.
[6] V. Uhnevionak et al., Mater. Sci. Forum 778-780, 483 (2014).
[7] S. K. Haney, S-H. Ryu, S. Dhar, A. Agarwal, and M. Johnson, *MRS Proceedings*, vol. 1069, 2008.
[8] A. Agarwal and S. Haney, Journal of Electronic Material, 37 (5), 646 (2008).
[9] S. M. Sze, *Physics of semiconductor devices*, 2nd ed.,. New York: Wiley, 1981.
[10] S. Potbhare, N. Goldsman, and G. Pennington, J. Appl. Phys. 100, 044515 (2006).