Bodo´s Power Systems®

Power Cycling Community 1995-2014

An overview of test results over the last 20 years

Semiconductor lifetime is a key factor for economical and sustainable use of power electronics. To assess the lifetime of power electronic modules, active power cycling tests are a state-of-the-art procedure. This article shows the results of 110 publications from the last 20 years related to samples per test run, temperature swing, coolant temperature and cycling time.

By Aaron Hutzler, Felix Zeyss, Stephan Vater, Adam Tokarski, Andreas Schletz and Martin März,
Fraunhofer Institute of Integrated Systems and Device Technology, Nuremberg, Germany

Manufacturers of power semiconductors and modules invest much money and effort into the optimization of their products' reliability. This includes predicting in-application lifetime through active power cycling tests. To distinguish various products and technologies, these tests have to be comparable in terms of parameters, conditions and results.

This study analyzed correlations and mismatches between 110 publications of the power cycling community. Due to the lack of a complete description of boundary conditions, test strategy, and end of life criteria, only 59 papers were usable for the comparison. However, the remaining papers nevertheless exhibited a huge variety.

Active Power Cycling Tests

Active power cycling determines lifetime of power modules under working conditions. The modules are mounted on a heat sink (cooling with air or liquid) and a voltage is applied in forward direction to reach a defined current. This current through the Device Under Test leads to power loss and results in an increase of the semiconductor temperature. When the current is periodically switched on and off the temperature of the semiconductor rises and falls due to alternating heating and cooling. One power cycle is defined as the full period of heating up the junction from minimum temperature $T_{j,Min}$ to maximum $T_{j,Max}$ and cooling it down. In most test setups, the temperature and electrical data are monitored during each cycle. If these values changed more than a previously determined amount (e.g. 20 %), the end-of-life criteria is fulfilled [52].

The number of cycles to failure (N_f) is mostly influenced by the temperature swing at the junction (ΔT_j), the minimum temperature ($T_{j,Min}$), the heating time (t_{on}), and the current (I_{Heat}) [13; 63]. Besides these obvious influences, the mounting of the device on the heat sink (i.e. thermal resistance and thermal impedance) also influences power cycling results. Another factor is the size and type of the semiconductor device, which has to be considered when separating different product families and generations.

In conclusion, power cycling tests can lead to a lifetime approximation which is close to the application when performed under realistic conditions. Power cycling can be distinguished from the passive temperature cycling test in terms of heating source (active vs. passive). Furthermore, the commonly used cycle times are about ten to hundred times shorter at power cycling than at temperature cycling (seconds vs. minutes).

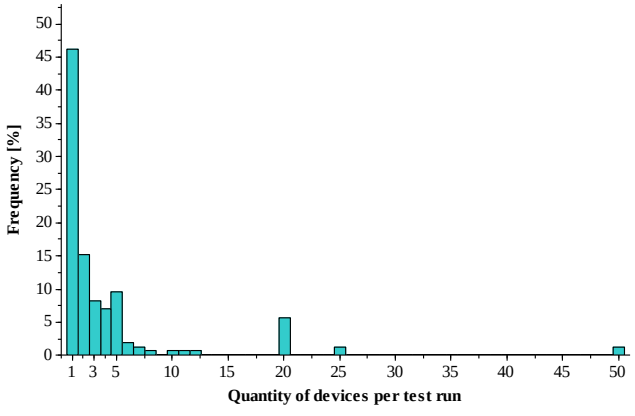

Figure 1: Histogram of samples per test run [1–65]

Reviewed Papers

This study analyzed publications from 1995 to February 2014, which dealt with the topic active power cycling and/or semiconductor lifetime in general. Originally, 110 papers built the database. In the end, 59 of those papers contained usable information in terms of a complete listing of test conditions, as well as using a standardized test procedure (cooling method and cycle times). Yet, only a few papers stated the basic conditions. For example, the number of samples was missing quite often. Figure 1 shows the distribution of the devices per test run.

For any paper with no given number of devices, the sample size was assumed to be one. In order to recognize significant effects between different power cycling tests, the statistical power has to be known. This can only be achieved with an analysis, which requires a minimum of 10-15 samples per test. As there are minor deviations in the production parameters, the result for every sample can differ.

Regarding the test conditions, the analyzed papers showed a variety in terms of test setup, monitoring, and power-cycling parameters. This variety might be due to the fact that an international standard for power cycling tests does not exist. In fact, there are several standards that differ in regards to the main focus of the test [60–62].

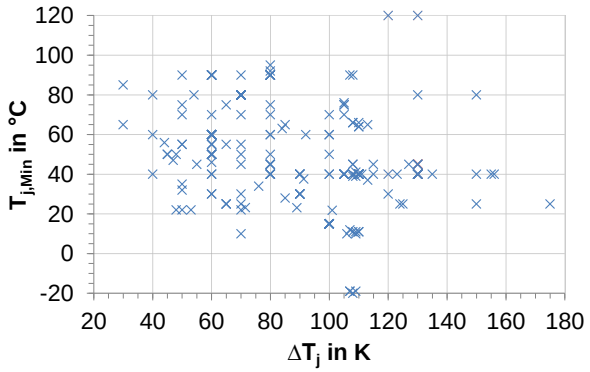

Figure 2: Minimum temperature versus temperature swing [1–3; 5; 7–15; 17; 18; 20–22; 24–40; 42–55; 57–59; 64]

Figure 2 illustrates the essential test parameters that could be extracted from the papers. The minimum junction temperature per test run is drawn versus the temperature swing of the device. The diagram shows that the majority of the tests took place in the temperature interval from 20 °C to 90 °C and temperature swings from 40 K to 110 K. There are only a few tests with temperature swings higher than 110 K and minimum temperatures below 40 °C. For modern semiconductor materials (e.g. SiC) as well as modern joining technologies a higher temperature range is of interest. Studies showed that increasing the coolant temperature can have a positive impact on application lifetime [30]. Thus, the test temperatures for future standards and publications should be extended.

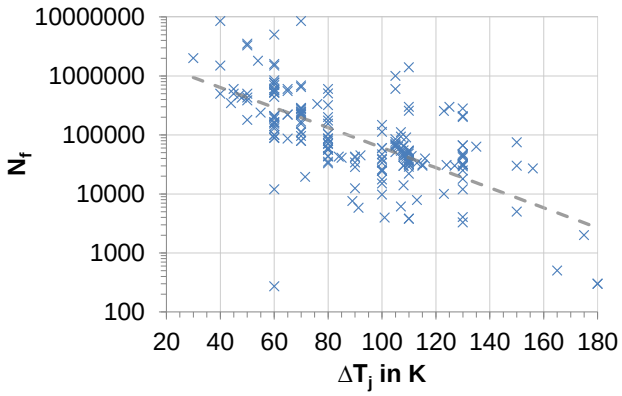

Figure 3: Number of cycles versus temperature swing [1; 3–5; 8–11; 13–25; 27; 29–34; 36; 37; 40; 43–45; 47–59; 64]

Power Cycling Test Results

To see any influences of the test parameters on the lifetime, the results of the individual test runs have to be taken into account. This analysis is limited by the fact that many different devices' test results had been published and no common test standard was given. Furthermore, the observable dependence of the lifetime on any factor is influenced by the variation of other factors.

An exemplary dependency analysis can be seen in Figure 3. It shows the cycle count to failure versus the temperature swing of the device. A dependency is visible, indicated by the dotted line. This corresponds with the empirical lifetime curves of power semiconductors, for which the following dependency was found: $N_f \propto \Delta T_j^{-\beta_1}$ [13; 63, 65].

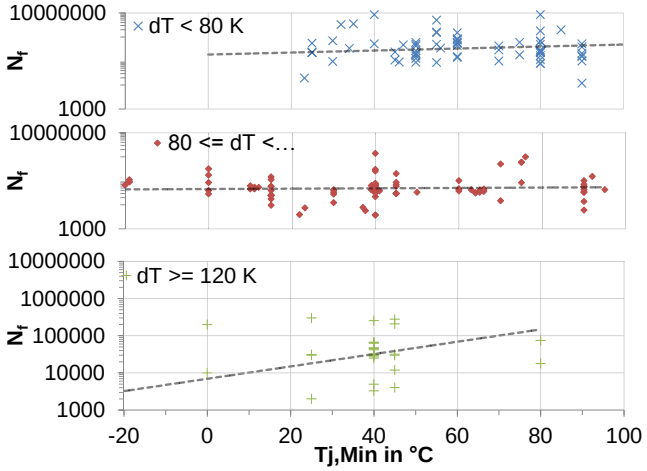

Figure 4: Number of cycles versus minimum temperature [1; 3; 5; 8–11; 13–15; 17; 18; 20–22; 24; 27; 29–34; 36; 37; 40; 43–45; 47–55; 57–59; 64]

When compared to the minimum junction temperature, the achievable cycle count does not show any significant dependency, as seen in Figure 4. In the observed temperature range, $T_{j,Min}$ has a much lower influence on lifetime than the temperature swing.

In the previously mentioned lifetime models, the influence of the coolant temperature is given by an Arrhenius-term:

$N_f \propto \exp\left(\frac{\beta_2}{T_{j,Min} + 273}\right)$ [13; 36; 63].

In this case, empirical lifetime curves predict a lower lifetime at increased temperatures, which did not correspond with the analyzed data.

Another factor that is supposed to influence the number of power cycles is the timespan in which the device is powered on and conducts current. Figure 5 shows the achieved power cycles per test versus the used on-time.

The cycle time seemed to influence the lifetime, but the data set was quite low compared to the last diagrams, which meant that the result was less reliable. This comes from the fact that the value of the heating time ton was missing quite often. However, most papers did

state the cycle time without mentioning the ratio of on- and off-time (symmetrical $t_{on} = t_{off}$ or asymmetrical $t_{on} \neq t_{off}$.). It should be stated that the heating time has a too high influence to neglect.

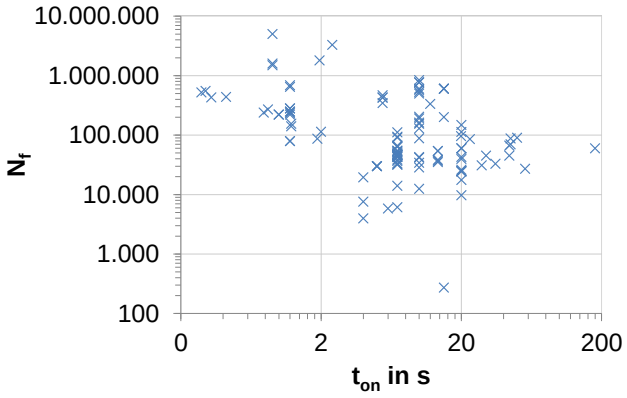

Figure 5: Number of cycles versus heating time (IGBT only) [1; 4; 5; 8; 10; 11; 13–18; 20–22; 24; 27; 29–34; 36; 37; 40; 43–45; 47; 49–59]

Conclusion and Outlook

The study showed that an international standard for active power cycling tests is needed. The lack of complete data regarding the test strategy, conditions, number of devices, and sample setup makes most results not reproducible at all. Almost every institution that deals with semiconductor reliability has developed its own internal procedures.

A suggestion could be the harmonization of the cooling method or the mounting of the samples. Furthermore, a detailed list of essential test variables has to be stated in the conclusion. To end this diversification in test procedures, a newly revised and internationally accepted standard is inevitable. Otherwise the published data will remain worthy for marketing purposes only for all future.

Note: This study makes no claim to be complete. The shown overview will be continuous improved and new or not included papers are welcome.

References are listed at Fraunhofer

www.iisb.fraunhofer.de/pct