Developing Digital Test Sequences for Through-Silicon Vias within 3D Structures

Matthias Gulbins, Fabian Hopsch, Peter Schneider, Bernd Straube, Wolfgang Vermeiren

Fraunhofer IIS/EAS Dresden, Germany

Contact: {matthias.gulbins | fabian.hopsch | wolfgang.vermeiren}@eas.iis.fraunhofer.de

Abstract—Through-silicon vias (TSVs) present new, essential elements within 3D stacked Integrated Circuits (IC). Since they connect different layers of 3D stacks, their proper operation is an essential prerequisite for the system function. In this paper a procedure for deriving local digital test sequences for TSVs is presented. The behavior of TSVs including their typical surrounding circuitry is investigated under the impact of assumed faults using fault simulation. Since a purely digital consideration of faulty behavior of TSVs is not sufficient, the TSVs have to be modeled and analyzed at electrical level. The TSVs are embedded by inverters used as drivers at the inputs and buffers at the outputs. All mentioned elements are described at electrical level by spice-like netlists. By an analogue fault simulation tool faults are injected into this electric network model. The simulations of the so modified networks were running in parallel on a compute cluster including the evaluations of the fault effects. The fault simulations are carried out automatically. The test signals needed for fault detection are concatenated to form a digital TSV test sequence.

Index Terms—3D IC testing, TSV test, test sequences for TSVs, defect-oriented testing, electrical level fault simulations

I. INTRODUCTION

The technology of three-dimensional (3D) integration of Integrated Circuits (IC) by means of through-silicon vias (TSVs) opens up new opportunities for system realization. Benefits are primary reduced footprint, shorter wire length, and smaller size (form factor). This leads to higher performance, smaller power dissipation, and finally to lower manufacturing costs compared to a SoC realization [1]. However, there are enormous challenges regarding the technology itself as well as design and test issues. Thermal, power, and infrastructure difficulties have to be mastered before 3D IC industrial production will be feasible [2]. Therein, 3D IC testing is considered as the 'No.1 challenge' of all the design, tool, and methodology challenges in the 3D IC field [3]. Resulting from the insufficient understanding of 3D testing issues and the lack of Design-for-Test (DfT) solutions the launch of the 3D technology is complicated [4]. The main test challenges and the need for new methods for testing of 3D ICs have been summarized in [5][6] and [7], respectively. New approaches for test signal generation are necessary. They also have to be targeted to TSV interconnect test.

Within 3D stacked ICs, TSVs present new, essential elements. By the use of this new type of interconnections of the various tiers it is expected to substantially improve interconnect bandwidth. However, the test approaches have to target 3D specific defect mechanisms [8] because 3D IC manufacturing comprises processing steps which are considerably different from those in the 2D IC case. Thus, due to the extra 3D specific processing steps such as thinning, alignment, and stacking, it is necessary to take new fault models into account and derive appropriate tests for these new interconnect elements [1].

The following defect mechanisms have been identified as particularly appearing for 3D: voids, peeling, delamination, chipping, and cracking. They arise from several reasons and can lead to imperfect via connections up to random open defects [6][8]. They have been characterized in [9] as the defect types 'hard/weak opens' and 'hard/weak shorts'.

But, not only new defect mechanisms require the test of the TSVs. To guarantee the full functionality and reliability of 3D TSV interconnects, designers must take the precaution and implement redundancy and self-repairing mechanisms for TSVs [8][9]. This requires as essential part the test of the TSVs to identify the faulty ones and replace them by fault-free ones using appropriate rerouting strategies. Due to insufficient test accessibility of the TSVs, DfT approaches as described in [1][10][11] are crucial. Local digital test sequences are also needed to test circuits designed considering DfT.

A straightforward built-in self-test approach [12] detects faults appearing as hard opens or hard shorts between neighboring TSVs. But delay or sequential faults can be detected by chance only. On-chip sense amplification regards a TSV as a resistance-capacitance combination and detects faults if its time response significantly changes [13]. When including TSVs into DRAM's fault mechanisms, opens are detected, which occur on TSVs as part of the wordlines and the bitlines of the whole stacked DRAM [14]. In [15] the test of pinholes of TSVs focuses to shorts from the TSV to substrate.

Although the TSVs are essential for the 3D technology, only a few papers deal with the test of TSVs in detail. Most authors involved in the design of 3D circuits regard the TSV as connection with digital features.

In this paper a procedure for deriving test sequences for TSVs based on fault models at electrical level is presented. Defects can be modeled in more physical detail at this level. With this, on the one hand, defective effects which cannot be described at logic level can be detected. On the other hand, information about fault sizes and their interrelation to tolerable operation limits can be obtained. For providing such a test derivation an electrical level fault simulation tool will be used.

The remainder of the paper is organized as follows. After a short outline of modeling of TSVs, the electrical network model used for the investigations is presented in section II. The subsequent section describes the generation of the test sequences. Section IV outlines the fault simulation procedure for investigating the behavior of TSVs under the impact of faults. In section V results regarding fault detectability and the required tests are depicted. The paper concludes with summary and outlook.

II. MODELLING OF THROUGH-SILICON VIAS

TSVs connect different dies of a 3D stack. Generally, models of the TSV are used for simulating its behavior. The approach to test development for the TSVs in this paper requires a model of them at electrical level.

The authors in [16][17][18] employ analytical models, considering mainly resistances of the via and capacitors to substrate. These models are applied to compute the propagation delay of TSVs [16] or to estimate the scaling trend of characteristic parameters [18]. Electrical models are needed for more detailed studies. To investigate RF characterization, a π - spaced equivalent model is employed containing resistors, an inductor, and capacitors [19]. For examining signal integrity issues and signaling techniques for TSV interconnects, a model of two coupled TSVs at electrical level is applied [20][21]. It includes additionally coupling capacitances and inductances.

The authors of [22] model and simulate parasitic effects in stacked silicon. These effects occur especially on neighboring TSVs. An electrical model of two neighboring TSVs is derived. All models of TSVs at electrical level differ to minor degree only. The model of [22] is chosen and extended to three neighboring TSVs (cf. Fig. 1).

Each TSV is modeled by a network as shown in Fig. 1. Each TSV is coupled with the substrate via a capacitor and a conductor. Additionally between the middle points of two neighboring TSVs an equivalent electrical circuit exists representing the coupling of the corresponding TSVs. To cover a wider range of structural details of TSVs and technology properties, based on this generic structure a refinement of the network model topology as well as the consideration of further physical effects can be carried out. The approach described in the following is suitable for all these TSV models.

Mostly there exist drivers and buffers separating the TSVs from the other parts of the circuit, e. g. flip-flops of a scan path. This is also valid in case of self-repair mechanisms where multiplexers are applied. Therefore drivers and buffers, both realized as inverters, are included [20][21]. The drivers are located at the bottom and the buffers at the top of each TSV. Thus, the signal directions are from bottom to top. The circuit to be investigated consists so of three neighboring TSVs, each driven by a driver and examined by a buffer.

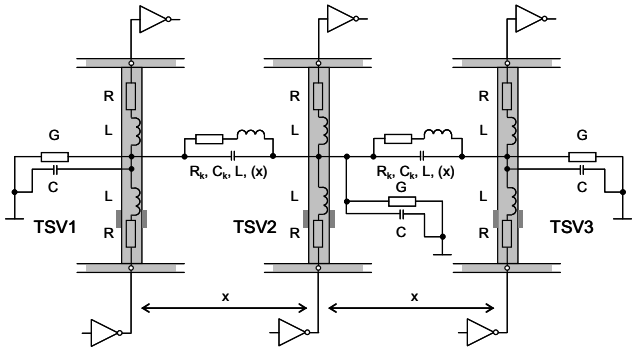

Fig. 1. Equivalent electrical circuit of three neighboring TSVs.

III. GENERATION OF TEST SEQUENCES

The test generation based on the electrical model of the TSV described in section II is performed by using fault simulation. Defect impacts can be modeled at electrical level with a high accuracy. The results are mapped to gate level. Thereby the provided test sequences can be applied for tests at gate level but with a rating relative to defect impacts at electrical level. Exhaustive test sequences are deployed to provide a rating for all possible test sequences.

In the fault simulation process faults are injected into the model of the TSVs and test sequences are applied. Using a set of faults and a set of test sequences, a fault detection matrix (FDM) is provided. It exhibits which faults are detected by which test sequences or alternatively which test sequence detects which faults.

These test sequences applied by the fault simulator are the input for the test generation. During the test generation process test sequences are selected, compacted, and concatenated to form the entire test sequence.

Test sequences with a length one are required to detect combinational faults whereas test sequences with a length n are needed to detect sequential faults of depth n-1. In this paper test sequences with a length two are provided. This restriction of the sequential depth simplifies the procedure of test generation. Principally, faults with larger sequential depth can be detected by this approach.

Single test sequences are concatenated in an arbitrary order to form the entire test. As a prerequisite the single tests must be independent of the preceding sequence, especially they must not rely on the initial state of the circuit during simulation [23]. This is guaranteed if two test sequences that distinguish in the first bit only detect the same fault. The first bit can be omitted reducing so the length of the single test. If e. g. the tests 001 and 101 detect the same fault, then the sequential test 01 is

sufficient to detect this fault. Generally, this rule can be applied consecutively.

In order to handle tests of sequential depth two, exhaustive test sequences of length three are applied. From the results of the simulations, single test sequences of length two or combinational tests are deduced by the above rule. Tests which cannot be deduced are not regarded here. They give hints to faults which need tests with higher sequential depth. This step of reducing the FDM results in a modified fault detection matrix (mFDM).

Furthermore the content of mFDM has to be mapped to the fault locations. The resulting fault value matrix represents relations between fault location and fault size.

The results concerning test sequences are mapped to gate level for the use within digital test.

IV. FAULT SIMULATION

A Analogue Fault Simulator aFSIM

Fault simulation is applied for different tasks e.g. fault detection, determination of fault coverage, and the development of tests. Furthermore diagnosis tasks can be solved using fault simulation. In fault simulation faults are injected into a model of a circuit. Faults are generated concerning a set of fault models and a model of this circuit. Fault models represent the behavior of defects arising during production or operation of a circuit.

Fault simulation can be applied at different levels of abstraction. In this paper fault simulations are executed at electrical level. For this purpose the fault simulator aFSIM [24] is deployed. It is capable of utilizing several network simulators like SPICE, Spectre, Eldo or TITAN (Infineon). In Fig. 2 the fault simulator aFSIM is depicted schematically. For running fault simulations an electrical description of the circuit in form of a netlist is needed. Further, a fault list with |F| entries, a list of parameter vectors for characterizing variations of component parameters with |P| entries, and a list of test sequences with |S| entries can be defined. Here, the simulations are carried out with the parameter set of the nominal circuit. Finally, an evaluation criterion must be defined.

After the definition of the input data each entry of the three lists is taken element wise and automatically set in the netlist. The input signals are set according the entry of the list of test sequences. The values from the entry of the list of parameter vectors are applied to the parameters and a fault is injected corresponding to the current item of the fault list. This results in |S|·|P|·|F| modified netlists. The simulations of the modified netlists are automatically distributed and run in parallel using available compute servers or a HPC-Cluster. The results of the simulations are evaluated according to the evaluation criterion. The outcome of the evaluation is stored in a database.

B Fault Simulation of TSVs

The model of the TSV from section II is embedded into a surrounding area for fault simulation. At each inverter directly connected to a TSV an additional inverter is appended. At input side at the bottom the additional inverter is added before the driver and at output side at the top after the buffer.

For the investigations transient simulations are utilized. As test sequences exhaustive sequences with a length three are applied. This results in $2^3 \cdot 2^3 \cdot 2^3 = 512$ test sequences, because a circuit with three TSVs is used. Each part of a test sequence is applied for 1 ns, representing a clock frequency of 1 GHz. The test sequences are modeled with piecewise linear sources with a signal transition time of 20 ps. High level voltage amounts to 1.1 V. Only nominal values for each parameter are employed.

Faults are injected into the TSVs and into the inverters that are directly connected to the TSVs. The single fault assumption is made. In the TSVs opens and shorts are expected. Opens are

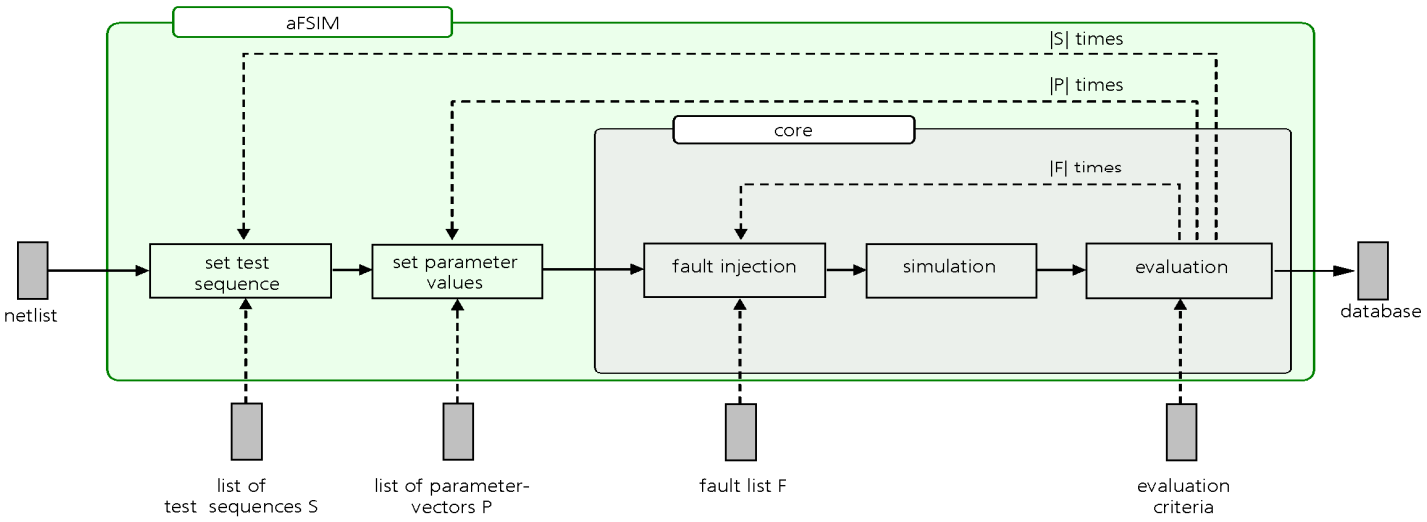

Fig. 2. Diagram of the fault simulator aFSIM.

modeled by replacing each resistor R with highly resistive resistors. Ten different values are used ranging from 10 kΩ to 1 GΩ. Shorts are modeled by injecting resistors between neighboring TSVs using ten different resistors from 1 Ω to 100 kΩ. The values of the faults are based on [9]. Shorts are assumed between the top, the middle, and the bottom point of two neighboring TSVs. For the 12 fault locations this results in 120 faults.

Opens and shorts are also injected into the drivers and buffers. It is assumed, that these inverters belong to the TSVs and are not tested by single die testing. Extracted netlists [25] are used for the inverters. Opens are modeled by replacing parasitic line resistors with highly resistive ones. Shorts are set between the connections of each transistor. Each considered inverter comprises 22 fault locations. For the faults within the inverters the same values for the fault models as for the TSVs are utilized. This modeling results in 1,440 different faults, 120 faults within the TSVs and 1,320 faults within the inverters. Although the drivers and buffers have more than ten times as many faults as the TSVs, they are needed, because they form a unit with the TSVs and enable their test.

The evaluation takes place at the output side of the buffers. The evaluation criterion relates to the deviations between the output voltage curves of the simulations of the fault-free and the faulty circuit. To define the evaluation criterion all test sequences have to be examined for the fault-free circuit regarding the propagation delay. In the worst case the propagation delay is about 320 ps. The evaluation interval begins at 400 ps of the last part of a test sequence and persists to the end of the simulation. A fault is marked as detected, if the absolute value of the difference between the outputs of the faulty and the fault-free netlist is larger than 0.8 V in the evaluation interval. A detection of a fault at the primary outputs of a circuit is confident using an absolute deviation of 0.8 V since the high level voltage amounts to 1.1 V.

The number of test sequences is 512, and the fault list contains 1,440 different faults. This results in 512·1,440 = 737,280 modified netlists. The simulations of the modified netlists are automatically distributed on a HPC-Cluster with 128 processors. It takes about 34 hours running all simulations. The results of the fault simulations are stored in a database.

V. RESULTS

The regarded faults of the TSVs and the drivers and buffers are opens and shorts. Considering the analogue character of these faults it is obvious that their effect depends on the real resistance. Opens with low resistance are no opens, but with high resistance. It is the goal of our investigations to show at each fault location which resistors lead to a detectable fault and which not. The ten different resistors of each fault location were selected so that both detectable and undetectable faults occur.

The fault simulation procedure delivers for each fault the detectability with regard to the applied test sequences. This results in the FDM. The FDM created here has 1,440 lines representing the faults and 512·3 = 1,536 columns representing the test sequences combined with the three observed outputs. A cell of this matrix contains a ‘1’ if the corresponding fault is detected with the related test sequence at the accordant output and a ‘0’ if not.

In the next step the large FDM is reduced by eliminating the influence of the preceding sequence. By this the test sequences will be independent from the simulator. This procedure has been described in section III. So the FDM is processed to create a new modified matrix mFDM representing test sequences of length two. It consist of 1,440 lines and 64·3 = 192 columns. An extract of the corresponding mFDM is depicted in Table I. Detected faults are marked by a green (light) and undetected by a red (dark) cell.

Table I is explained by some examples: Fault no. 18 is an open at the bottom of the left TSV with 100 MΩ. It can be detected, e.g. by the test sequences no. 40, 45, 46, 47 and 48 at output 1. Fault no. 61 is a short between the bottom side of the left and the middle TSVs with 1 Ω. It can be detected, e.g. by the test sequences no. 45 and 46 at output 1 and by no. 43 and 44 at output 2. The faults no. 110 and 676 cannot be detected using the given test sequences.

The original FDM reveals that 992 faults can be detected; the mFDM has 943 detected faults. 49 faults, all located within

Table I. Extract of a modified fault detection matrix mFDM.

Output	OUT1										OUT2										OUT3									
No. of Test Sequence / No. of Fault	40	41	42	43	44	45	46	47	48	49	40	41	42	43	44	45	46	47	48	49	40	41	42	43	44	45	46	47	48	49
18																														
61																														
77																														
110																														
486																														
676																														
765																														
820																														
1122																														
1337																														

Table II. Fault detection for selected sets of faults.

Set of Faults	# Faults	# det. Faults	# undet. Faults
TSVs	120	81	39
INVs	1320	862	458
TSV1 & app. INVs	460	295	165
TSV2 & app. INVs	460	311	149
TSV3 & app. INVs	460	295	165
Opens	1020	625	395
Shorts	420	318	102

inverters, have a higher sequential depth than one. In Table II the detectable und undetectable faults in the mFDM are summarized.

Finally, the results of fault simulation are regarded with respect to the fault locations as described in section III. The fault value matrix in Table III shows the fault locations of the TSVs and which values of resistors will be detected as faults. The upper part of the table corresponds to the opens within TSVs and the lower part to the shorts between neighboring TSVs. A line represents a fault location while the columns represent the different values that are used for the faults. A green (light) cell marks that at the corresponding fault location and value the fault is detected by a combinational test; blue (grey) by a sequential one. Red (dark) stands for not detected.

Table III shows that in case of shorts the fault detection at a TSV is mostly independent from its position, TSV1-TSV2 and TSV2-TSV3 have the same result independently whether bottom, middle, or top position. All shorts with values of 1 kΩ or lower are detected by combinational tests, shorts with 5 kΩ by sequential tests, whereas shorts with values of 10 kΩ or higher are not detected.

Contrary to shorts, opens have a heterogeneous appearance. Opens located near to output are only detected at high resistance, since the output buffers refresh also weak signals. So, opens below a resistance of 5 MΩ cannot be detected. Opens with 10 MΩ are detected by sequential tests and above 50 MΩ by combinational tests.

Opens concerning the bottom resistor are detected above 5 MΩ by combinational tests, with 500 kΩ by sequential tests, and not detected below 100 kΩ. If the resistance is 1 MΩ, TSV1 and TSV2 show different fault detectability. For TSV1 and TSV3 the faults are detected by combinational, for TSV2 by sequential tests.

Similar tables also exist for the drivers and the buffers.

VI. SUMMARY AND OUTLOOK

Test development in the field of emerging 3D structures was supported by an application of electrical level fault simulation. In this paper a procedure to derive digital test sequences for TSVs was presented. Exemplarily, a model of three neighboring TSVs was used. Faults were modeled at electrical level taking possible defects of the TSVs and the surrounding drivers and buffers into account.

As a result the created FDM illustrates which faults can be detected by which sequence of input signals. The FDM was processed to create a mFDM relative to test sequences of length two. With respect to the faults, the simulations demonstrate for different fault types and fault locations which resistance values lead to detectable faults. Finally, digital tests were derived which allow for detecting possible defects of the TSVs. The results exhibit that a large amount of faults cannot be detected by voltage comparison. These faults need further investigation because they can lead to reliability problems. Possible solutions could be IDDQ-Test or a test at various voltage levels.

For the investigations a model of three neighboring TSVs was employed. For generalizing analyses, investigations have

Table III. Fault value matrix representing relations between fault locations and fault sizes.

Value of Fault / Fault Location	10 kΩ	100 kΩ	500 kΩ	1 MΩ	5 MΩ	10 MΩ	50 MΩ	100 MΩ	500 MΩ	1 GΩ
OPEN TSV1 Top										
OPEN TSV1 Bottom										
OPEN TSV2 Top										
OPEN TSV2 Bottom										
OPEN TSV3 Top										
OPEN TSV3 Bottom										
Value of Fault / Fault Location	**1 Ω**	**10 Ω**	**50 Ω**	**100 Ω**	**500 Ω**	**1 kΩ**	**5 kΩ**	**10 kΩ**	**50 kΩ**	**100 kΩ**
SHORT TSV1-TSV2 Bottom										
SHORT TSV1-TSV2 Middle										
SHORT TSV1-TSV2 Top										
SHORT TSV2-TSV3 Bottom										
SHORT TSV2-TSV3 Middle										
SHORT TSV2-TSV3 Top										

to be carried out for further TSV configurations. Structures with higher numbers of TSVs comprising e.g. two border and more than three inner TSVs should be an appropriate next step to generalize this approach. This configuration includes the not yet examined cases of an inner TSV with two other inner TSVs as neighbors as well as an inner TSV with one border TSV and one inner TSV as neighbors. This is investigated in [26] together with a description of the possibility to calculate minimal combinations of test sequences for covering all detectable faults. Furthermore, a more detailed consideration of fault mechanisms in TSV w.r.t. to structural details and process properties must be included.

Finally, all these local tests have to be merged in order to form a test for all TSVs connecting the regarded tiers. Generally, the TSVs cannot be driven and buffered independently from each other, e.g. if they form a scan chain. This constraint has to be considered in test generation.

The presented procedure is prepared for taking process induced parameter variations of circuit components into account. Further work will support variation-aware test development for TSV-based structures. Wearout and aging effects will be investigated at electric level to support the development of tests for checking degradation impacts.

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