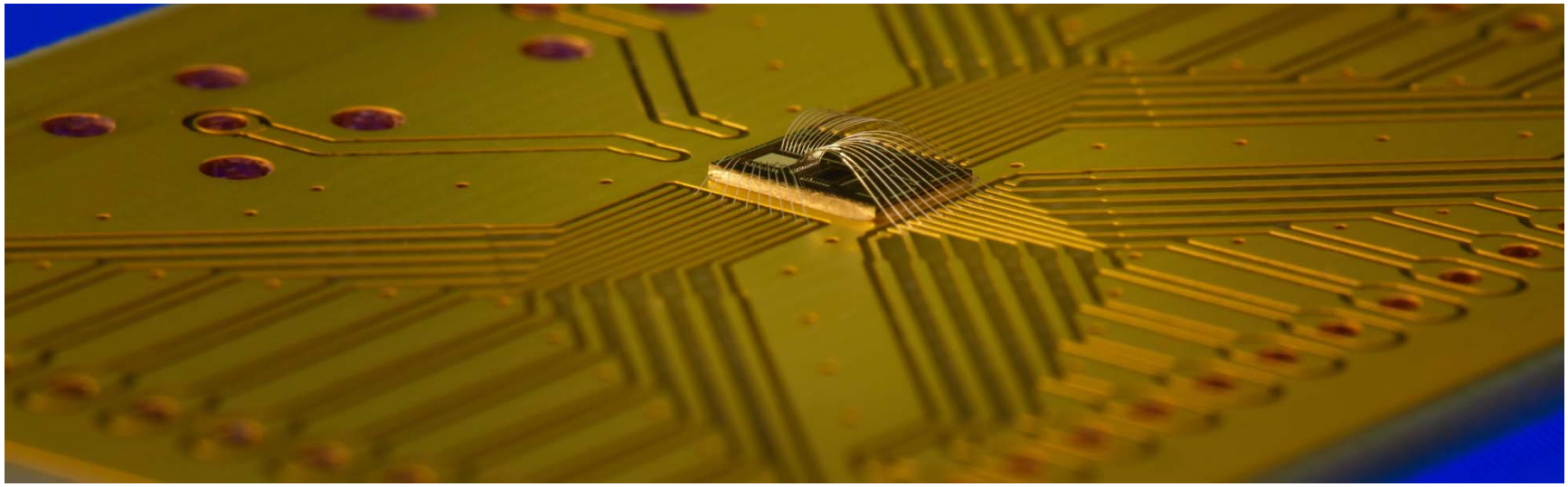
SILICON PROOF OF THE INTELLIGENT IP DESIGN FLOW

Using WiCkeD



Benjamin Prautsch
IC Design & Analog Design Automation

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Content

- Fraunhofer IIS/EAS – Mixed-Signal Design Service
- Mixed-Signal Design using Intelligent IP Design Flow
  - Key features
  - Automated Topology Selection using WiCkeD
  - Post Layout Optimization using WiCkeD
- Results
  - Mixed-Signal-IPs
  - Silicon Results
- Intelligent IP Design Flow for 28nm and below
- Summary

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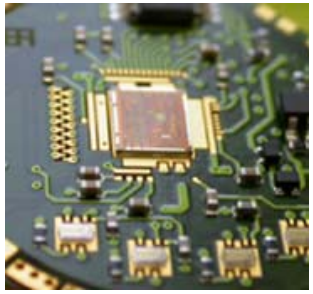
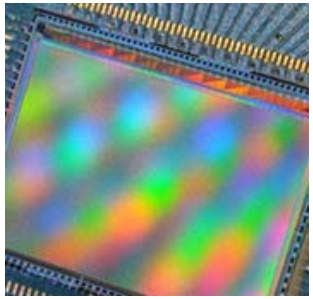
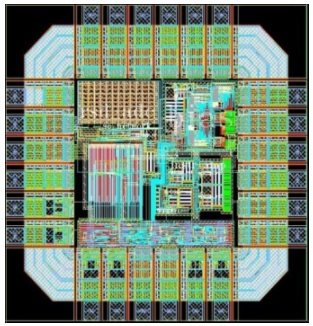
Design service for Mixed-Signal IP & ASIC
Our expertise

- Long-term experience in ASIC and IP design for …
  - embedded sensor, SMART sensor systems
  - Low-power (wireless) ASICs
  - automotive, medical, consumer electronics
  - RF and microwave applications
  - (optical) communication, CMOS image sensors
- Technology portfolio of 10+ foundries for feature nodes 0.6µm – 28nm







+ more efficiency and design safety due to Intelligent IP Design Flow

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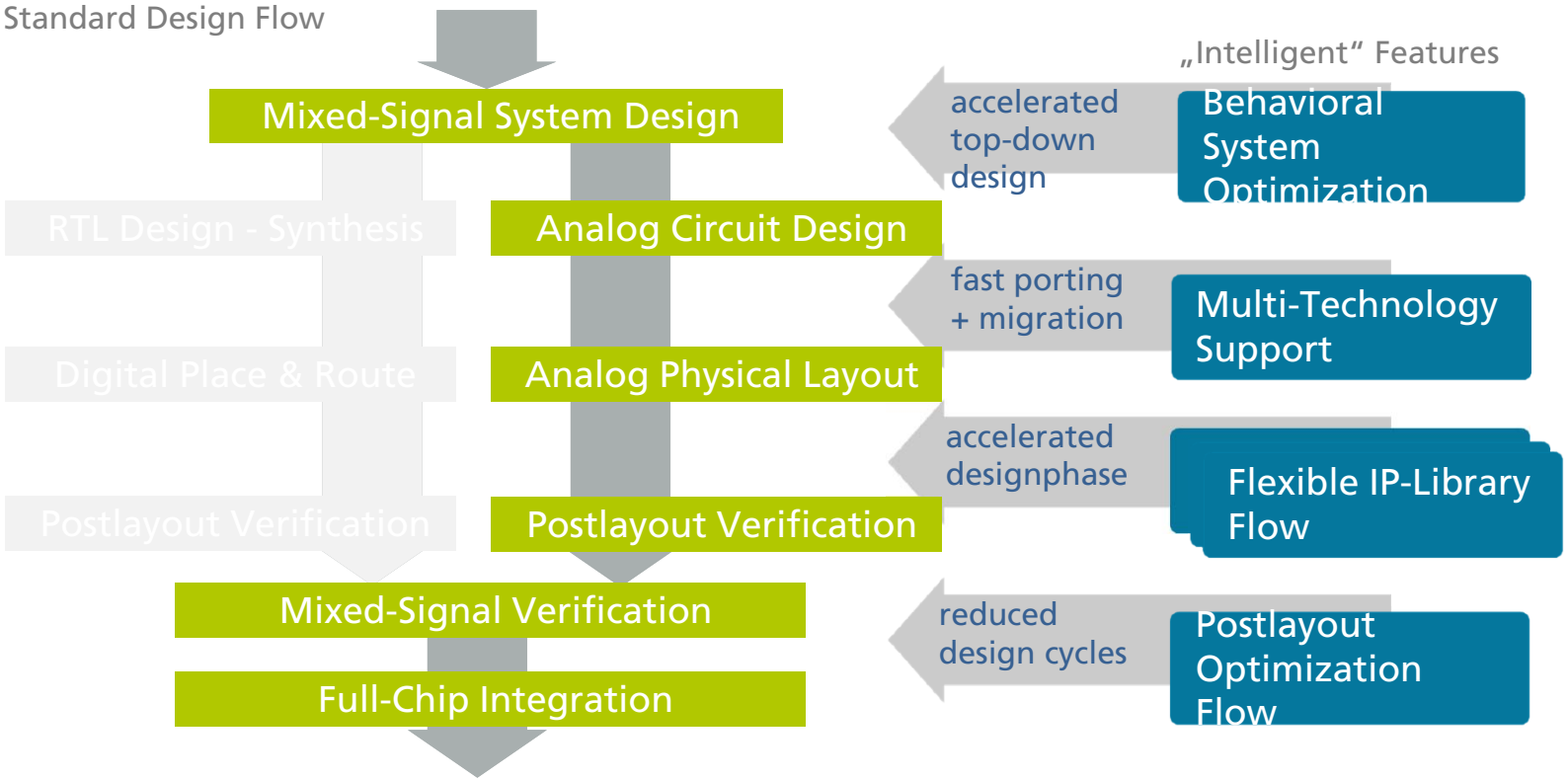
Intelligent Analog IP Design Flow

Motivation



- Typical procedure: handcrafted analog design
- Problem: slow, expensive, error-prone design; weak storage of knowledge
- Solution: novel Design Flow → faster, cheaper, more flexible, safer

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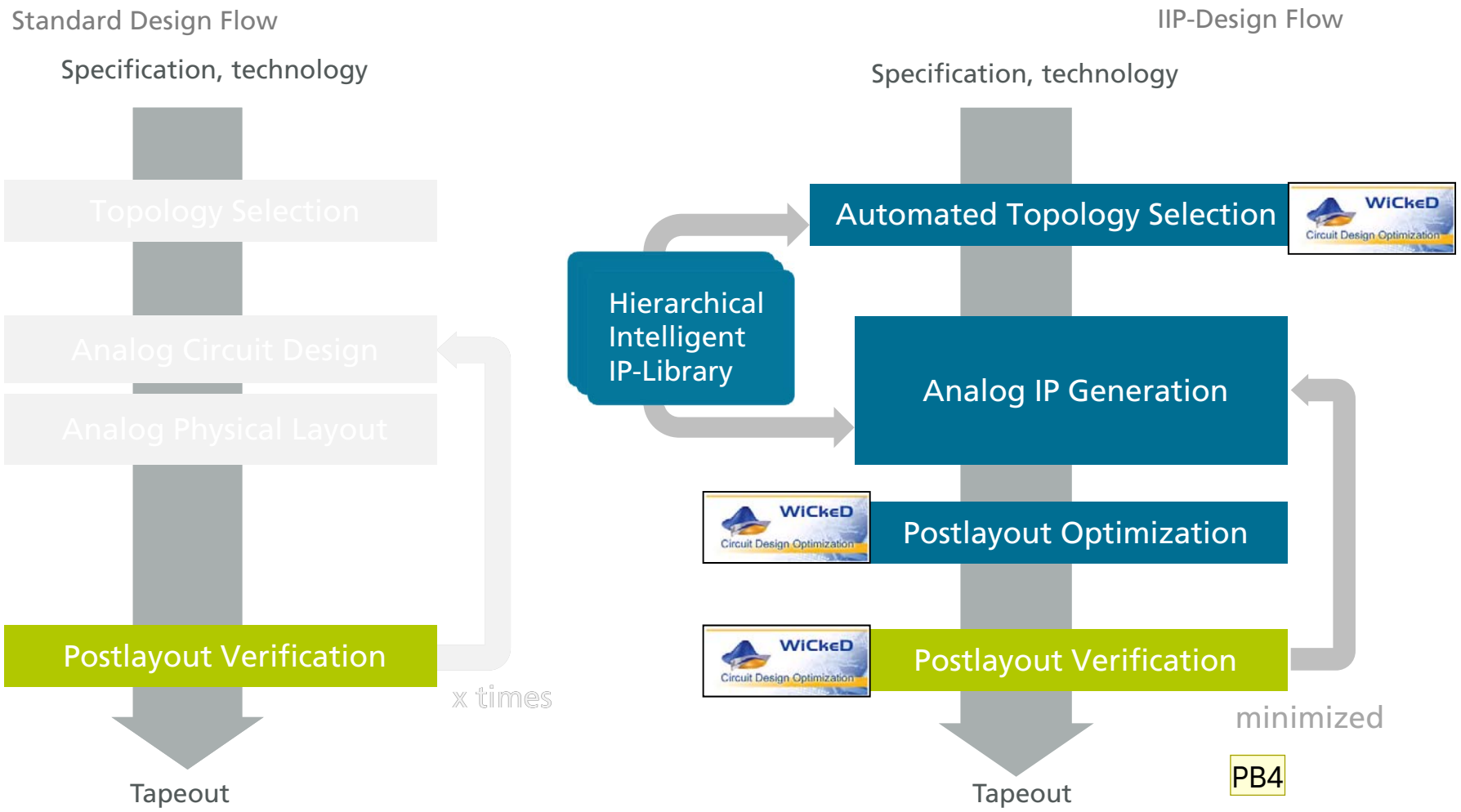
Intelligent Analog IP Design Flow

Key Features



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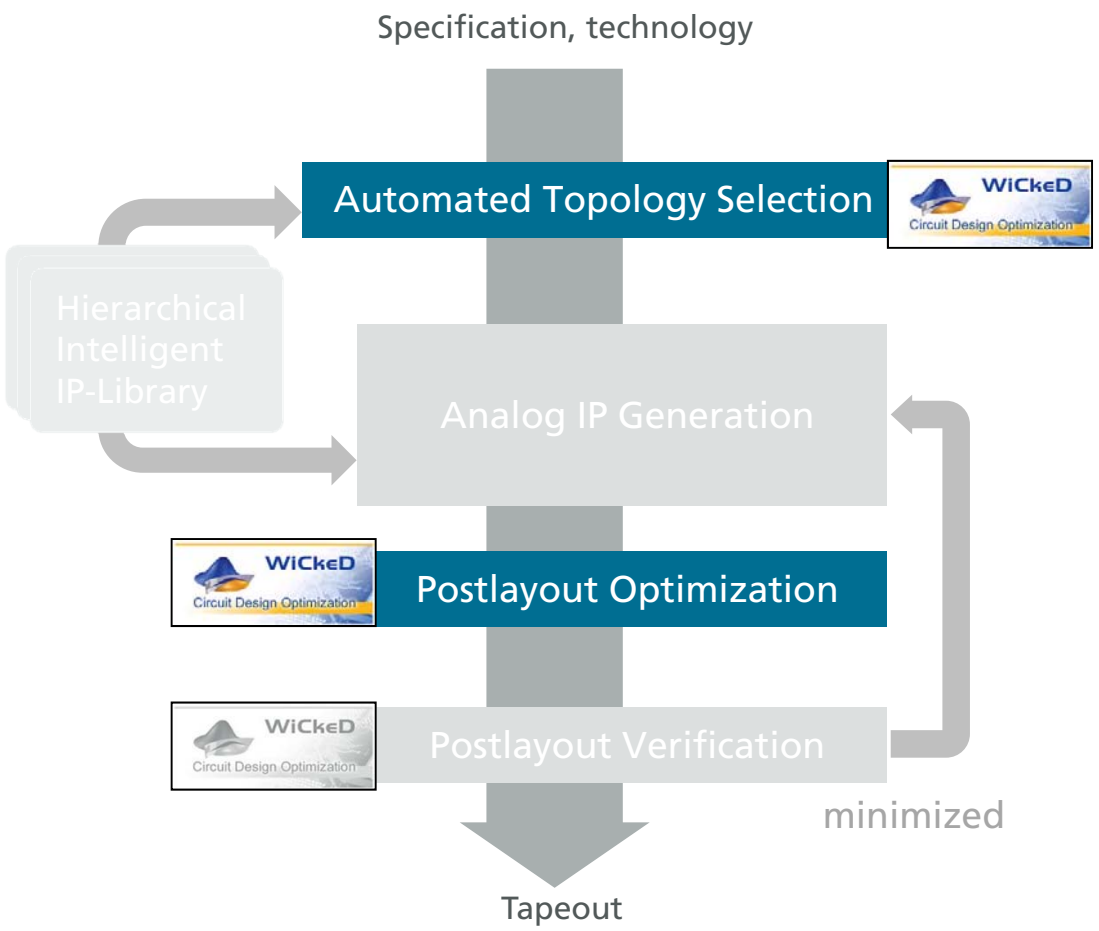
PB4 Wirklich minimiert?

Prautsch, Benjamin; 03.11.2014

Intelligent Analog IP Design Flow
Key Features using WiCkeD



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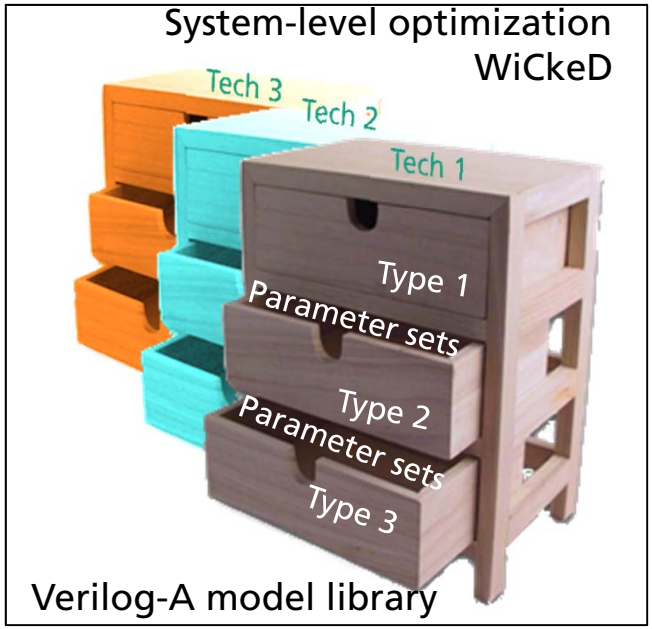
Intelligent Analog IP Design Flow
Automated Topology Selection

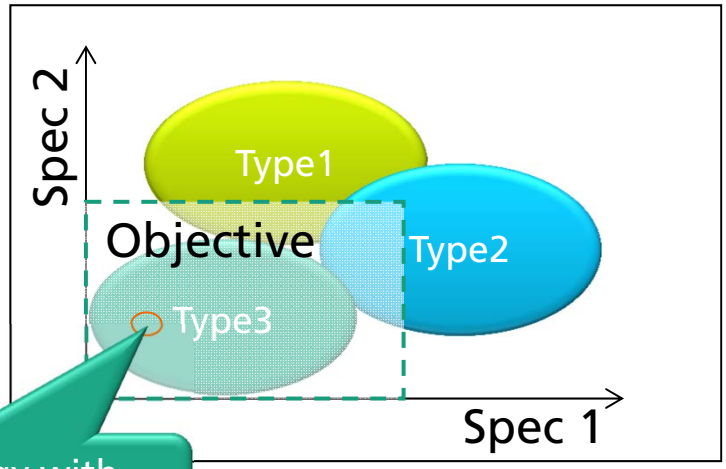
- Requirement: model + parameter definition
  - Generic model
  - Concrete parameters

PB2

- Input:
  - Specification
  - Technology

- Result of optimization
  - Block topology X with
  - Parameterization Y





Concrete Topology with Parameters will be selected

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Folie 9

PB2 würde das betonen:
- bisher vergleichsweise wenig auf diesem Gebiet
--> vorhandene Ideen nachnutzen

Prautsch, Benjamin; 30.10.2014

TR1 Abstrakter darstellen zum Verständnis

Torsten Reich; 30.10.2014

TR4

Intelligent Analog IP Design Flow
Postlayout Optimization

- Usage of commercial tools: Virtuoso or

- Back-annotation of extracted parasitics into schematic
  - Knowledge-based sensitivity-analysis of parasitics
  - Relevant, exact parasitics → efficiency vs. precision

- Parametric simulation with parasitics
  - Optimization including layout effects
  - Close-to-Silicon performance, no over-margin design→ Silicon Proven

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Folie 10

TR4 für MUGM überarbeiten

Torsten Reich; 30.10.2014

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Recent Mixed-Signal-IPs
Using Intelligent IP Design Flow & WiCkeD

IP-Name	Tech	IIP Design Flow	WiCkeD	Status
INSIDE180v1	180 nm	X	X	validated
INSIDE180v2	180 nm	X	X	validated
INSIDE180v3	180 nm	X	X	validated
INSIDE180v4	180 nm	X	X	validated
PIPEADC350v1	350 nm	X		validated
PIPEADC350v2	350 nm	X		validated
FlashADC180	180 nm	X		fabricated
CyclicFD180v1	180 nm	X	X	verified
CyclicFD180v2	180 nm	X	X	verified
SubBG180	180 nm	X		fabricated
SubBG350	350 nm	X		verified
StdBG180	180 nm	X		verified
SubBG040	40 nm	X		verified
SubBG028	28 nm	X		verified
FDOTA180	180 nm	X		fabricated

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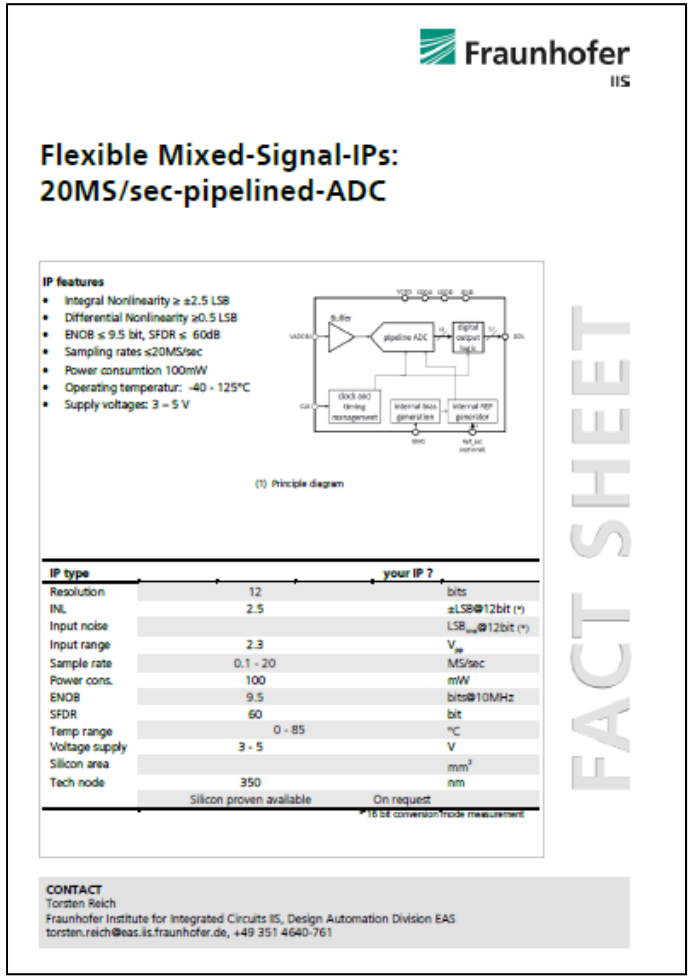
Mixed-Signal-IPs using Intelligent IP Design Flow

Silicon Results example 1: 20MS/sec-pipelined-ADC



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Flexible Mixed-Signal-IPs: 20MS/sec-pipelined-ADC

IP features

- Integral Nonlinearity ≥ ±2.5 LSB
- Differential Nonlinearity ≥0.5 LSB
- ENOB ≤ 9.5 bit, SFDR ≤ 60dB
- Sampling rates ≤20MS/sec
- Power consumtion 100mW
- Operating temperatur: -40 - 125°C
- Supply voltages: 3 – 5 V

(1) Principle diagram

IP type		your IP ?	
Resolution	12		bits
INL	2.5		±LSB@12bit (*)
Input noise			LSB_{rms}@12bit (*)
Input range	2.3		V_{pp}
Sample rate	0.1 - 20		MS/sec
Power cons.	100		mW
ENOB	9.5		bits@10MHz
SFDR	60		bit
Temp range	0 - 85		°C
Voltage supply	3 - 5		V
Silicon area			mm^2
Tech node	350		nm
	Silicon proven available	On request	

*16 bit conversion/node measurement

FACT SHEET

CONTACT
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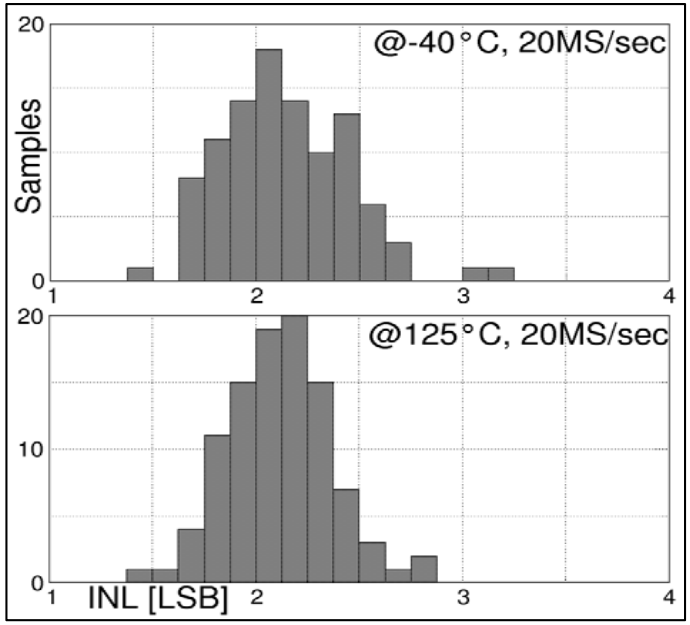
torsten.reich@eas.iis.fraunhofer.de, +49 351 4640-761

- Post Layout Yield Optimization



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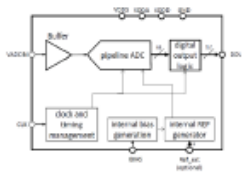

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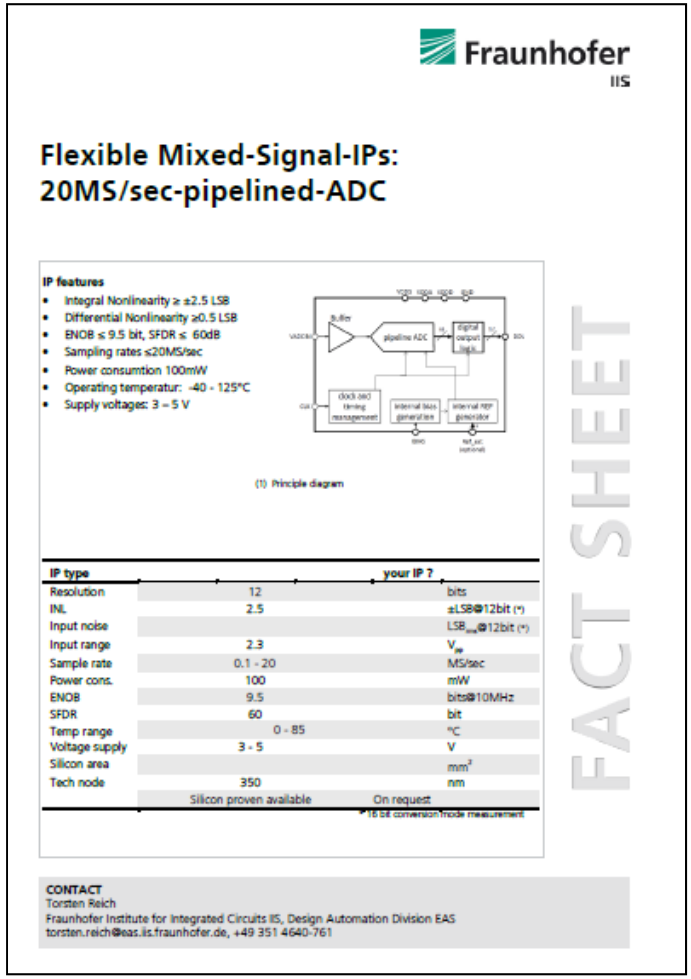

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- Close-to-Silicon Design (INL discrepancy < 0.2 LSB)
- Reduced design effort due to automated sub-IPs

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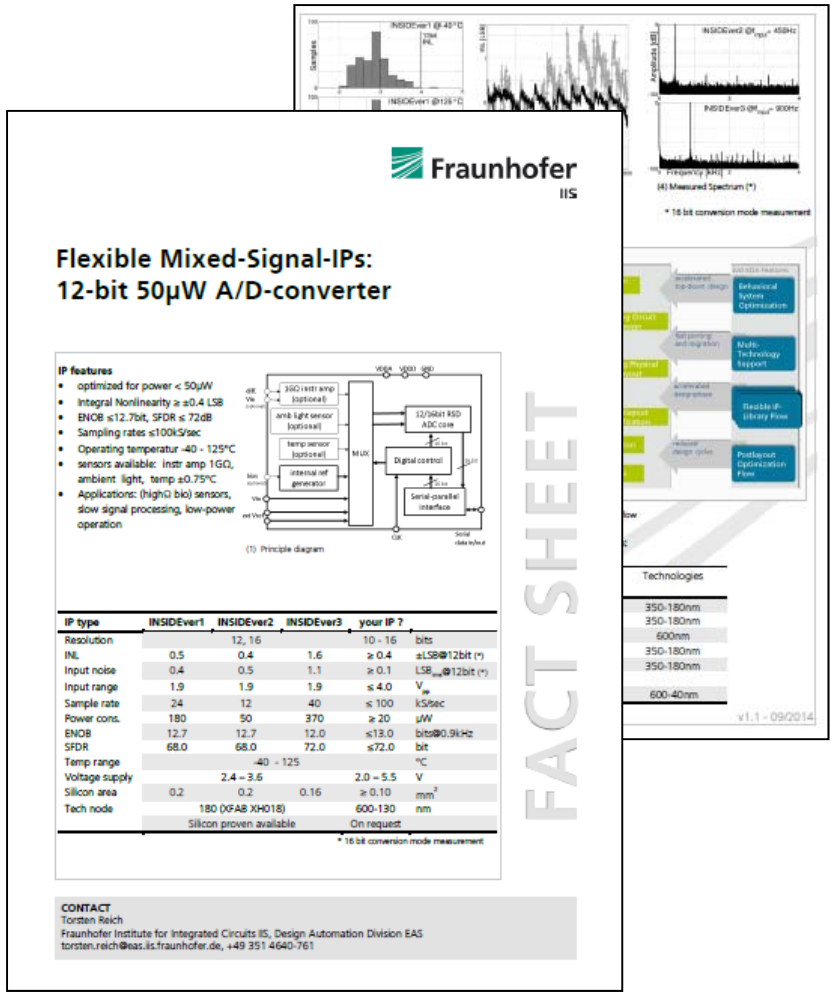
Mixed-Signal-IPs using Intelligent IP Design Flow

Silicon Results example 2: low-power 12-bit ADC



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Flexible Mixed-Signal-IPs:
12-bit 50µW A/D-converter

IP features

- optimized for power < 50µW
- Integral Nonlinearity ≥ ±0.4 LSB
- ENOB ≤12.7bit, SFDR ≤ 72dB
- Sampling rates ≤100kS/sec
- Operating temperatur -40 - 125°C
- sensors available: instr amp 1GΩ, ambient light, temp ±0.75°C
- Applications: (highΩ bio) sensors, slow signal processing, low-power operation

(1) Principle diagram

IP type	INSIDEver1	INSIDEver2	INSIDEver3	your IP ?	
Resolution		12, 16		10 - 16	bits
INL	0.5	0.4	1.6	≥ 0.4	±LSB@12bit (*)
Input noise	0.4	0.5	1.1	≥ 0.1	LSB_{rms}@12bit (*)
Input range	1.9	1.9	1.9	≤ 4.0	V_{pp}
Sample rate	24	12	40	≤ 100	kS/sec
Power cons.	180	50	370	≥ 20	µW
ENOB	12.7	12.7	12.0	≤13.0	bits@0.9kHz
SFDR	68.0	68.0	72.0	≤72.0	bit
Temp range		-40 - 125			°C
Voltage supply		2.4 – 3.6		2.0 – 5.5	V
Silicon area	0.2	0.2	0.16	≥ 0.10	mm^2
Tech node		180 (XFAB XH018)		600-130	nm
		Silicon proven available		On request	

* 16 bit conversion mode measurement

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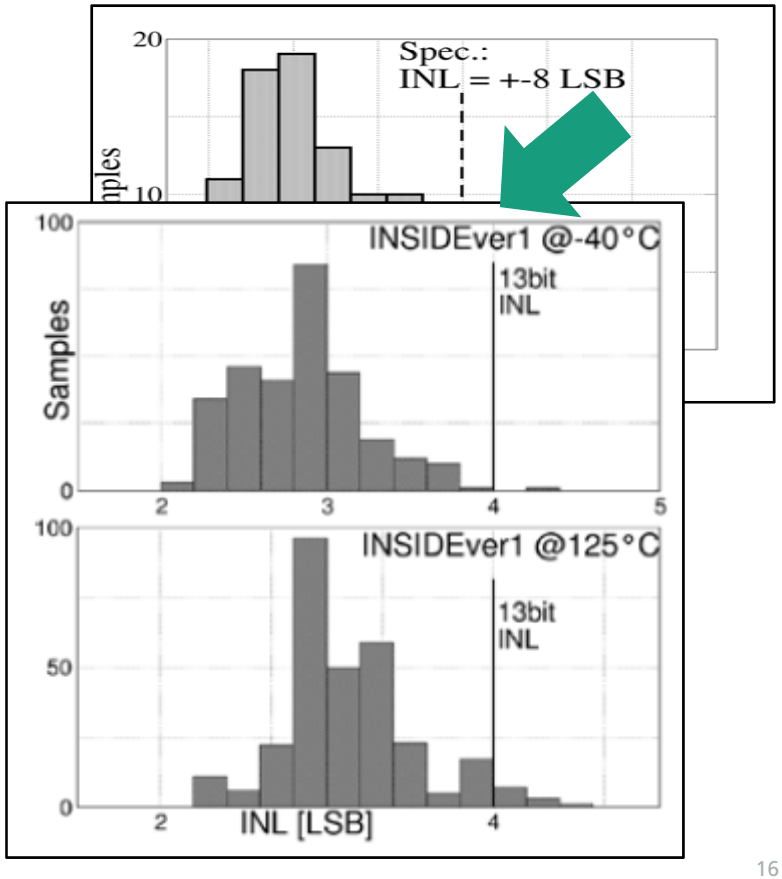

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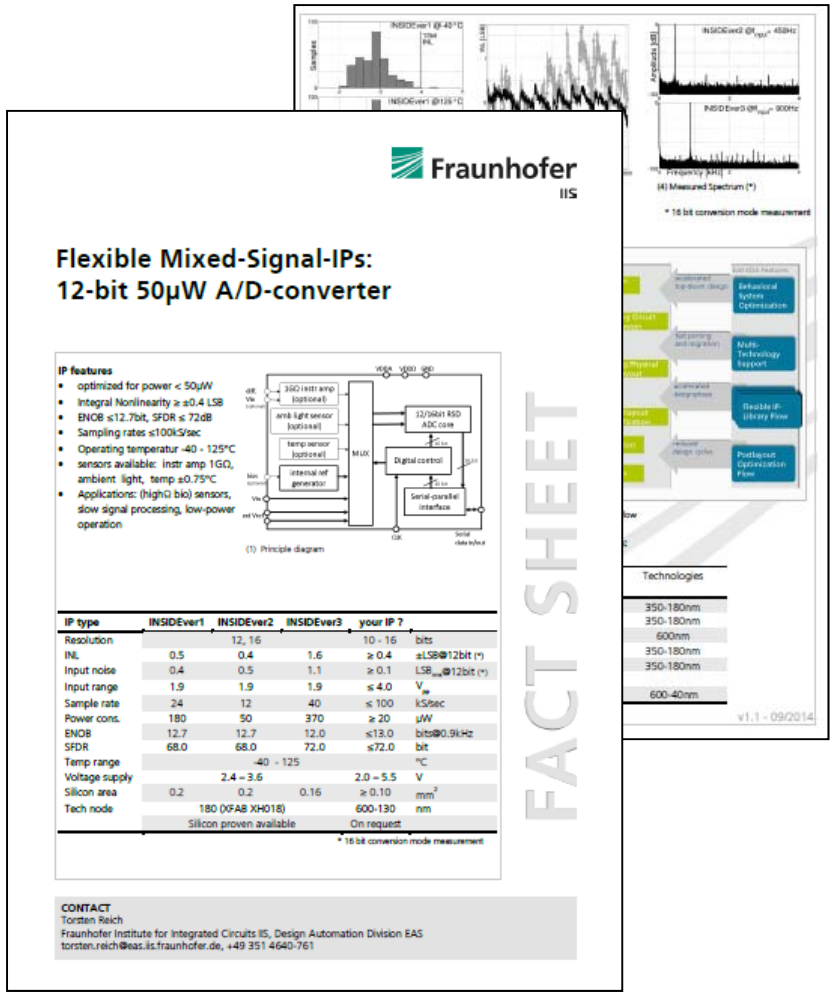
Mixed-Signal-IPs using Intelligent IP Design Flow

Silicon Results example 2: low-power 12-bit ADC



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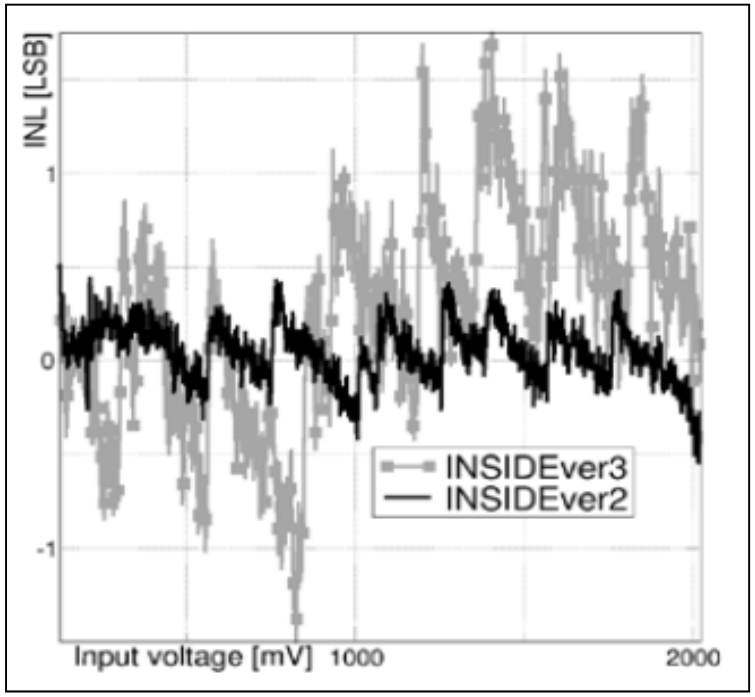

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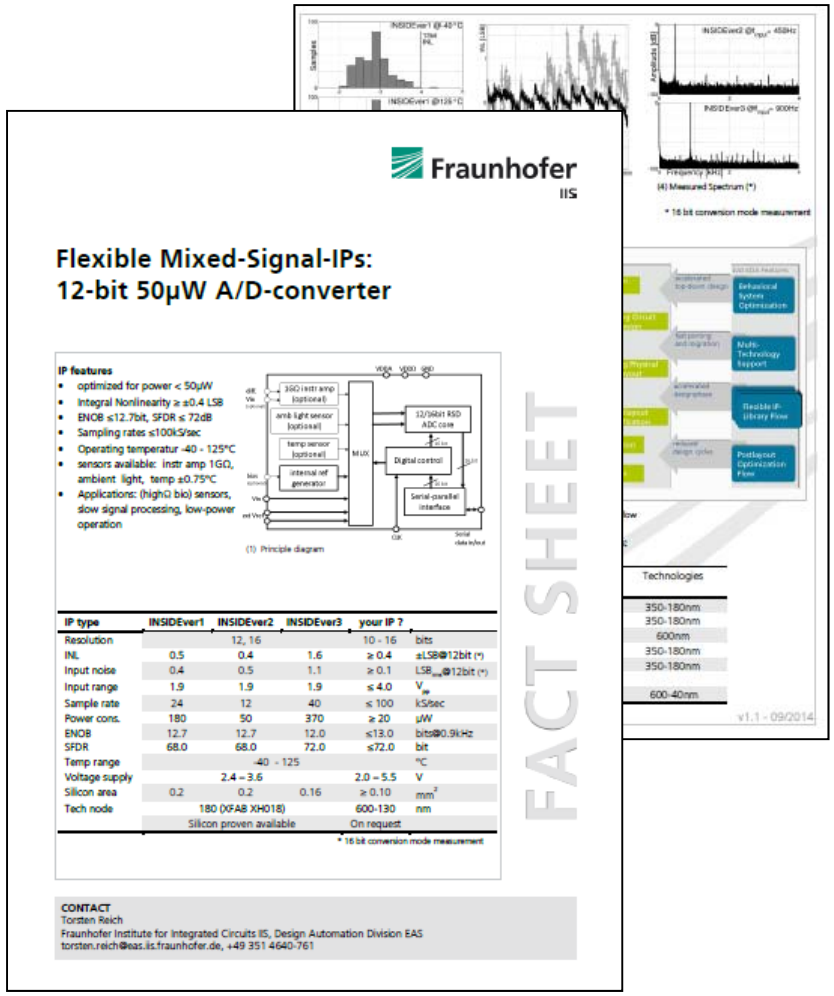
Mixed-Signal-IPs using Intelligent IP Design Flow

Silicon Results example 2: low-power 12-bit ADC



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- Close-to-Silicon-Design (INL discrepancy < 0.4 LSB)
- one flexible ADC-IP for 3 different specs
  - 40% more efficiency

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Silicon area	0.2	0.2	0.16

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Mixed-Signal-IPs using Intelligent IP Design Flow

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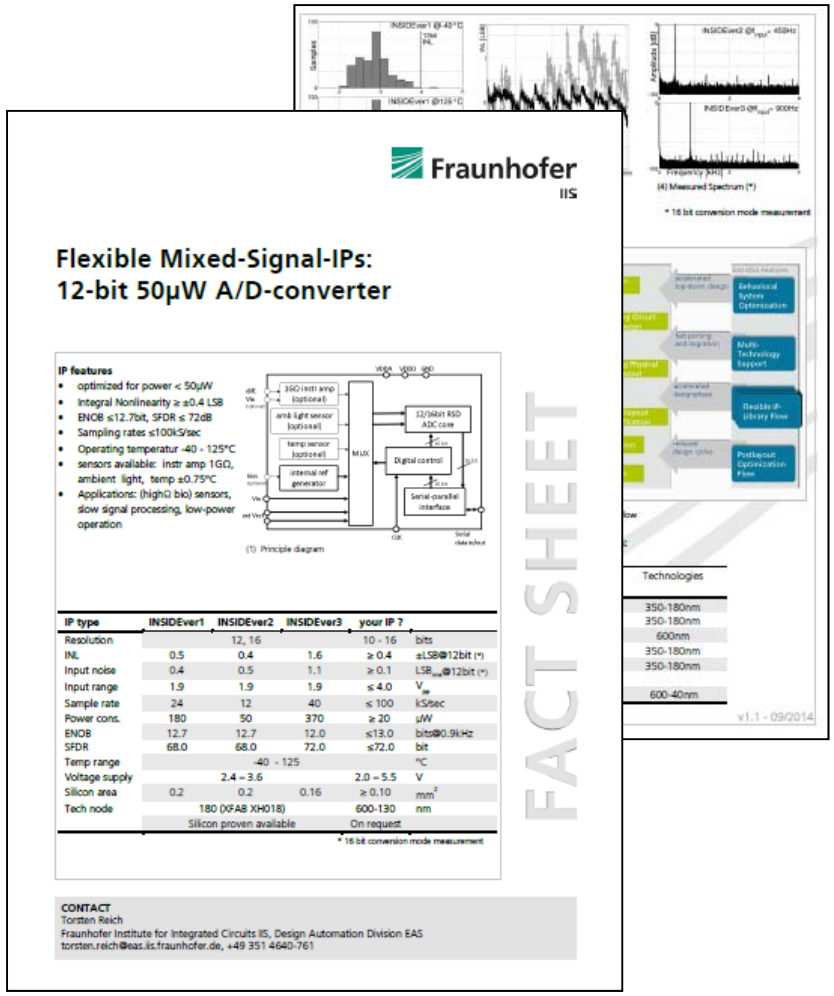

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SFDR	68.0	68.0	72.0	≤72.0	bit
Temp range		-40 - 125			°C
Voltage supply		2.4 – 3.6		2.0 – 5.5	V
Silicon area	0.2	0.2	0.16	≥ 0.10	mm^2
Tech node		180 (XFAB XH018)		600-130	nm
		Silicon proven available		On request	

* 16 bit conversion mode measurement

FACT SHEET

CONTACT
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- Post Layout Yield Optimization using WiCkeD
- Close-to-Silicon-Design (INL discrepancy < 0.4 LSB)
- one flexible ADC-IP for 3 different specs
  - 40% more efficiency
- Post Layout Verification using WiCkeD
  - -40..125°C validated
  - 2.4..3.6V supply validated

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Content

- Fraunhofer IIS/EAS – Mixed-Signal Design Service
- Mixed-Signal Design using Intelligent IP Design Flow
  - Key features
  - Automated Topology Selection using WiCkeD
  - Post Layout Optimization using WiCkeD
- Results
  - Mixed-Signal-IPs
  - Silicon Results
- Intelligent IP Design Flow for 28nm and below
- Summary

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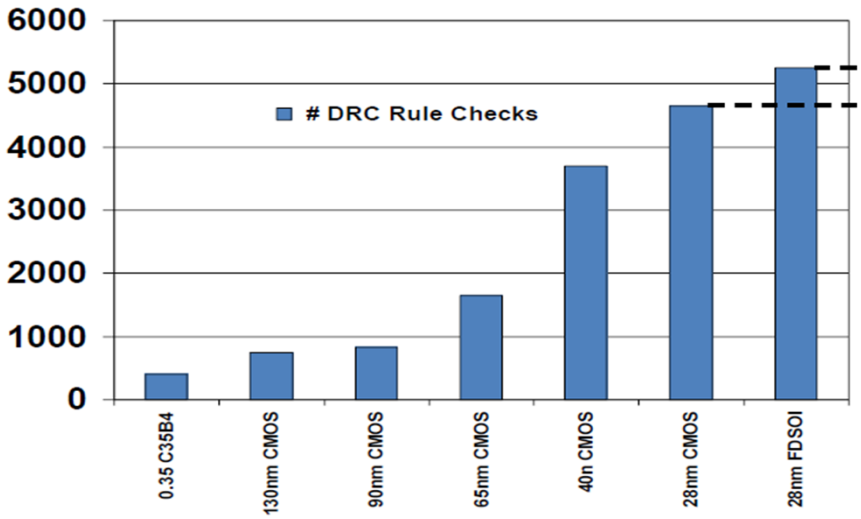
Intelligent IP Design Flow for 28nm and below
Introduction

- Complexity of small technology nodes
  - Strongly growing # of Design Rule Checks
  - Design rules depend on layout situation
  - Layout Dependent Effects



[STMicroelectronics, CMP annaual users meeting, 2014]

Layout-Dependent Effects	Prior to 40 nm	At 40nm	28nm and Beyond
Well Proximity Effect (WPE)	X	X	X
Poly Spacing Effect (PSE)		X	X
Length of Diffusion (LOD)	X	X	X
OD to OD Spacing Effect (OSE)		X	X

[Cadence, 2012]

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Intelligent IP Design Flow for 28nm and below
Current activities

- Intelligent IP Design Flow development for nanotechnologies
  - Flexible IPs for 40 nm & automated porting available
  - Flexible IPs for 28 nm bulk technology coming 2015
  - Development for 28nm FDSOI in progress
  - Development for 14nm FDSOI scheduled
- MunEDA is partner for WiCkeD integration into Intelligent IP Design Flow for overall feature size range

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Summary

- Fraunhofer IIS/EAS offers Mixed-Signal IPs & Design Service
  - Using Intelligent IP Design Flow
  - Up to 40% cost reduction proven
  - Close-to-silicon design validated
- MunEDA WiCkeD is prospective tool for
  - Automated Topology Selection
  - Post Layout (Yield) Optimization
  - Post Layout Verification
  - Porting Support
- Intelligent IP Design Flow in 0.6µm – 40nm is our State-of-the-Art …
  … our challenge is 28nm and below

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THANK YOU FOR YOUR ATTENTION

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Fraunhofer IIS MunEDA

WiCkeD-Trainingskurs

24. - 25.02.2015

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